Parallel Operation of GaN Power HEMTs

Overview

Power devices are connected in parallel to handle high currents when they cannot be supported by a single device or if it is more desirable to use two (or more) smaller devices. Ideally, we want devices in parallel to share at all times and hence we target a 50:50 split of the load in each device. In practice, devices in parallel do not share current and energy losses equally. In static operation, this is due to mismatches in device on state resistance, $R_{DS(on)}$. In dynamic operation, this is mainly due to mismatches in device threshold voltage, $V_{GS(th)}$ and gate charge, Q_G. In this application note, we focus on two GaN devices in parallel under hard-switching operation and investigate implications of device mismatches as well as operating temperature. Both simulated and measured test data is presented to show good correlation. It is shown that ICeGaN™ GaN HEMTs in parallel operate well in both static and dynamic conditions.

Contents

Nomenclature

C_{GS}	Gate–source capacitance
C_{GD}	Drain–gate capacitance
C_{DS}	Drain–source capacitance
C_i	Input capacitance of a power device
C_o	Output capacitance of a power device
d	Duty cycle
E_{off}	Energy loss in the channel of the switching device at its turn-off
E_{on}	Energy loss in the channel of the switching device at its turn-on
E_{on-Co}	Energy loss in the channel of the switching device at its turn-on due to the discharging of its C_o and the charging of complementary device's C_o under a fully hard-switched event
E_{on-VI}	Energy loss in the channel of the switching device at its turn-on due to external load current i_L
f_{sw}	Switching frequency
f_{sw}^*	f_{sw} below which two devices in parallel lower the overall power loss compared to a single device
i_{CH}	Channel current
i_{DS}	Drain–source current
i_L	External Load current
P_{con}	Conduction power loss
P_{QA}	Power loss in device Q_A when the two devices Q_A and Q_B are connected in parallel
P_{QB}	Power loss in device Q_B when the two devices Q_A and Q_B are connected in parallel
P_{sw}	Switching power loss
Q_1	Low-side device in half-bridge configuration
Q_2	High-side device in half-bridge configuration
Q_A, Q_B	Two devices connected in parallel
Q_{1A}, Q_{1B}	Two parallel devices at low side in half-bridge configuration
Q_{2A}, Q_{2B}	Two parallel devices at high side in half-bridge configuration
Q_G	Gate charge
$R_{DS(on)}$	On-state resistance of a power device
R_{GC}	Common gate resistance in driving two power devices connected in parallel
R_{G-on}	External gate resistance in the turn-on path
R_{G-off}	External gate resistance in the turn-off path
R_{load}	Load resistance connected between ground and the switching node
R_{senseA}	Sense resistance used to measure i_{DS} of Q_A
R_{senseB}	Sense resistance used to measure i_{DS} of Q_B
$R_{\theta QA,J-C}$	Junction to case thermal resistance of Q_A
$R_{\theta QB,J-C}$	Junction to case thermal resistance of Q_B
$R_{\theta QA,C-A}$	Case to ambient thermal resistance of Q_A
$R_{\theta QB,C-A}$	Case to ambient thermal resistance of Q_B
$R_{\theta,QA-QB}$	Thermal resistance between Q_A and Q_B when placed on a printed circuit board
T_{amb}	Ambient temperature
T_C	Device case temperature

ΔT_C	Difference in case temperatures between Q_A and Q_B
T_J	Device junction temperature
ΔT_J	Difference in junction temperatures between Q_A and Q_B
$v_{GS\text{-}internal}$	Internal gate–source voltage of an ICeGaN device
v_{DS}	Drain–source voltage
v_{GS}	Gate–source voltage (= external gate voltage for ICeGaN devices)
v_{sw}	Switch-node voltage in half-bridge configuration
V_{dc}	dc-link voltage
V_{DD}	Low-voltage supply to ICeGaN circuitry
$V_{GS(th)}$	Gate–source threshold voltage

1 Introduction

There is a continuous need to improve power density and efficiency of power converters as the global electricity consumption increases. A fundamental solution to this is to improve the performance of power semiconductor devices used in a converter by decreasing the on-state resistance ($R_{DS(on)}$) of the device for a given breakdown voltage. This can be effectively achieved in several ways. In conventional planar Si MOSFETs, $R_{DS(on)}$ has been reduced by improving the device design until the limit achieved by the particular technology [1]. Then a disruptive solution like super-junction technology brought further improvements to $R_{DS(on)}$ of Si devices with a major structural change to the design of conventional Si MOSFET [1]–[3]. The third method, which is to parallel two or more separate devices at board level, is used when a single device cannot handle the current demanded by high-power or large-load applications or there is an economic advantage to use two smaller devices over a single larger device.

With the advent of wide-bandgap (WBG) semiconductor technology, paralleling of WBG power devices is also sought after in order to go beyond the power density and efficiency limits reached by Si devices. **Figure 1(a)** shows a simple half-bridge configuration where Q_1 is the low-side device and Q_2 is the high-side device. In contrast, the half-bridge circuit in **Figure 1(b)** use two devices in parallel, both at low side (Q_{1A} and Q_{1B}) and high side (Q_{2A} and Q_{2B}). Ideally, provided that the circuit layout is fully symmetrical, the same principles apply for circuit operation where the two devices in parallel can be considered as a single device with lower $R_{DS(on)}$ (and higher capacitances). In reality, circuit layout will not be fully symmetrical, and more importantly, the two devices in parallel will have finite variations in their parameters such as $R_{DS(on)}$, gate charge (Q_G), and gate threshold voltage ($V_{GS(th)}$). These non-ideal factors demand special attention in circuit design, including gate driver selection and design, when paralleling is required. This is especially critical for WBG devices as they switch at much faster speeds compared to Si devices.

In this application note we will consider parallel operation of GaN power devices, focusing on CGD's 650-V 55-mΩ ICeGaN™ GaN power HEMTs [4], [5].

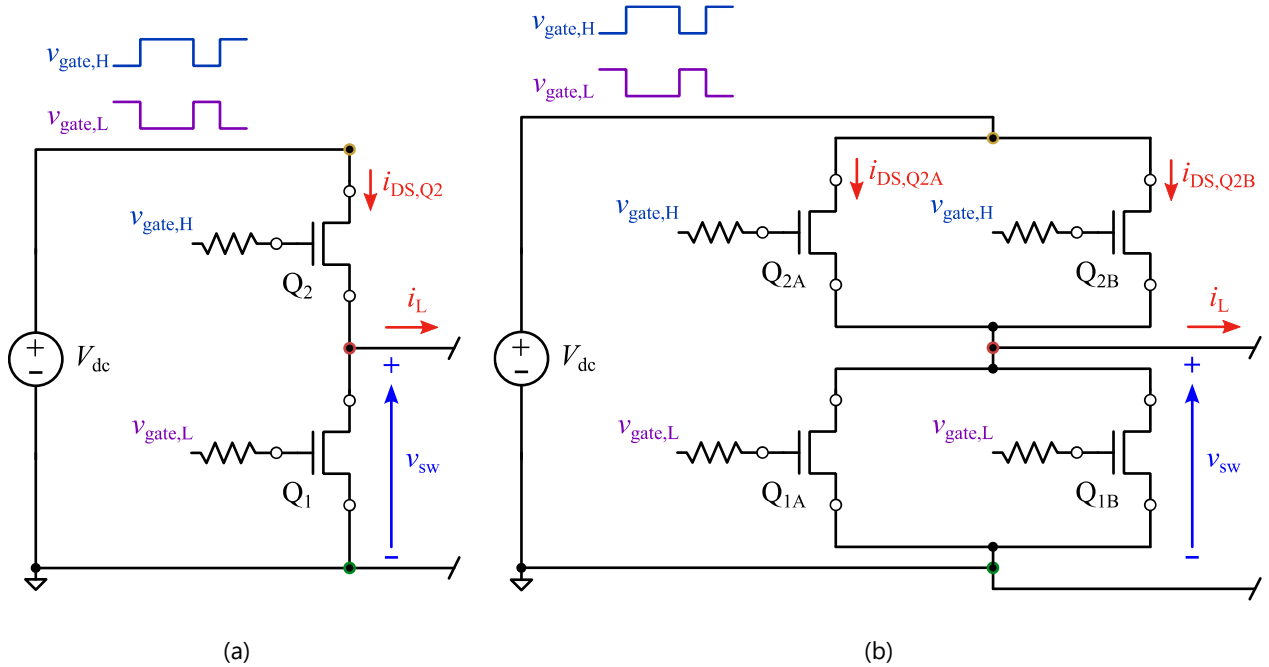


Figure 1 – Simple inverter leg arrangement with (a) single device in high and low sides and (b) 2x devices in parallel arrangement in high and low sides.

There are several technical aspects that need to be understood for parallel operation of power devices. These can be broadly categorized as follows and will be the subject of **Section 2**.

1. Power losses
2. Gate-driving requirements
3. Device parameters
    - Variation (determined by manufacturing process capability)
    - Temperature dependence
4. Circuit parasitics
5. Thermal considerations

Section 3 discusses parallel operation in practice. The chapter mainly focuses on the following two aspects considering both simulation and experimental results.

1. conduction (static) energy loss and sharing and
2. switching (dynamic) energy loss and sharing.

Two practical examples where ICeGaN devices operate in parallel are also presented.

Section 4 provides general design recommendations.

Finally, **Section 5** concludes the document.

2 Considerations in Paralleling Power Devices

This section discusses important considerations when paralleling power devices, accompanied by analytical and simulation results. First, a review on power loss calculations is given in **Section 2.1** to lay the platform for subsequent analysis.

Notes:

- We will consider hard-switching conditions in the following analysis. Concepts on static current sharing are applicable to soft switching as well. Most soft-switching circuits are zero-voltage-switched (ZVS) circuits and current and energy-loss sharing at the turn-on transition (discussed below) is not applicable to them as the devices are turned on at zero drain voltages. However, off-state losses [6] should be considered for soft-switching operation, and their effect on parallel operation is the beyond the scope of this application note.
- For definitions of the abbreviations or symbols used, please refer to the **Nomenclature** page.

2.1 Review on Energy Loss Calculation of Power Devices

Figure 2(a) shows an inductive-load circuit with two devices in half-bridge (or inverter leg) configuration. The low-side device Q_1 is switched with standard PWM switching and undergoes hard turn-on and turn-off transitions. The top device Q_2 is kept off and acts as a diode. The external load current i_L is considered to be a constant current equal to I_L.

The energy loss in the channel of Q_1 during its turn-on event is defined as the *turn-on energy loss* (E_{on}).

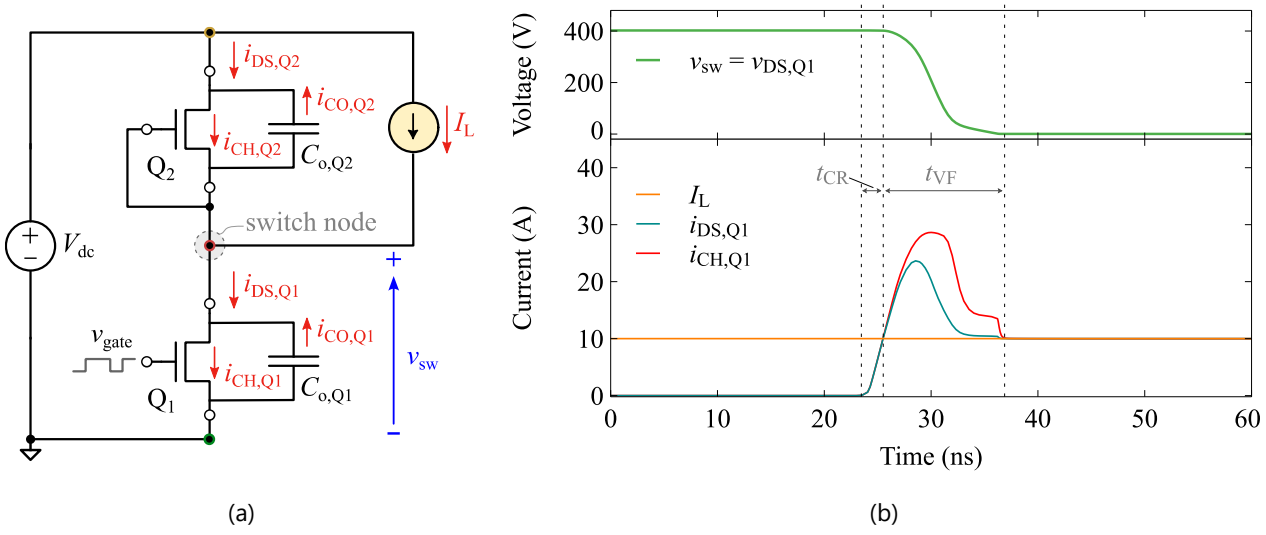
$$E_{\text{on}} = \int_{t_1}^{t_2} i_{\text{CH}} \cdot v_{\text{DS}}\, dt. \tag{1}$$

Here, the time period t_1 to t_2 denotes the duration of the on transition. Important waveforms related to the turn-on event of Q_1 are plotted in **Figure 2(b)**. E_{on} can be described as two loss components [6] as given by (2)–also see **Figure 3**.

$$E_{\text{on}} = E_{\text{on-Co}} + E_{\text{on-VI}} \tag{2}$$

1. The load-independent component $E_{on\text{-}Co}$.
   For a device undergoing a complete hard turn-on event, $E_{on\text{-}Co}$ is determined by the output charge (Q_o) of the device and can be calculated as follows [6]:

$$E_{\text{on-Co}} = Q_{\text{o}} \cdot V_{\text{dc}} = E_{\text{o}} + E_{\text{o}}^{*}. \tag{3}$$



(a) (b)

Figure 2 – (a) Inductive load circuit where the Q_1 is the main switching device (device output capacitance C_o is the parallel combination of C_{GD} and C_{DS}). (b) Simulation results showing important waveforms related to the hard turn-on event of Q_1.

$E_{on\text{-}Co}$ can be sepearated into two components: E_o, which is the energy stored in the device output capacitance, and E^*_o, which is the energy dissipated in the device channel due to the charging process of the complementary device's output capacitance [6]. As indicated by **Figure 3**, for a given dc-link voltage, $E_{on\text{-}Co}$ is independent of $R_{G\text{-}on}$. In practice, charge stored in parasitic capcitances of the PCB (switch-node to positive rail and switch-node to negative rail) and in inductors also contribute to E_{on} as load- and voltage-independent energy losses [7].

2. The load-dependent component $E_{on\text{-}VI}$.
   This is caused by the VI overlap of the external load current and the device drain–source voltage. As **Figure 2(b)** indicates, the overlap concerns the current rise time (t_{CR}) and the voltage fall time (t_{VF}). During t_{CR}, the load current I_L is shared between the drain currents of Q_1 and Q_2. During t_{VF}, the VI-overlap loss concerns the full load current. Therefore, the VI-overlap loss of Q_1 can be written as given by (4).

$$E_{\text{on-VI}} = \int^{t_{CR}} i_{DS} \cdot v_{DS}\, dt + \int^{t_{VF}} I_L \cdot v_{DS}\, dt \tag{4}$$

Figure 4 shows the variation of E_{on} with load current for two different turn-on gate resistance values: the higher the value of $R_{G\text{-}on}$, the higher the value of $E_{on\text{-}VI}$. This is because of the slowing of the discharge rate of device drain–gate capacitance that increases the duration of VI overlap of I_L and device v_{DS} [8].

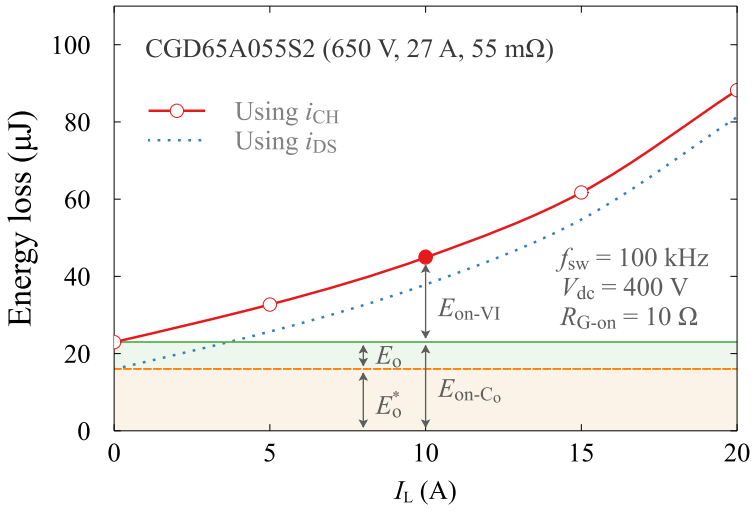


Figure 3 – The actual turn-on energy loss in device channel is calculated using channel current; use of drain current underestimates the turn-on energy loss. The variation is shown with load current.

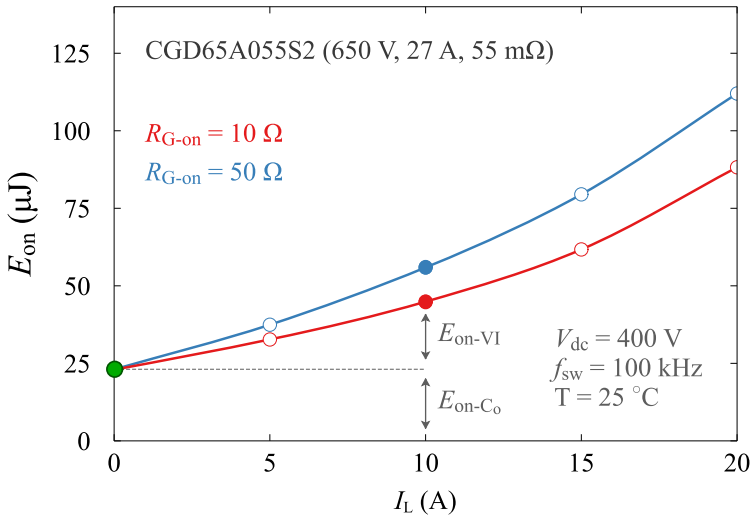


Figure 4 – Variation of turn-on energy loss in device channel with load current for different gate resistance values.

Referring to **Figure 3**, we observe that E_{on} increases with load current as the $E_{on\text{-}VI}$ increases, while $E_{on\text{-}Co}$ stays fixed for a giving dc-link voltage. The figure also explains why using the drain current to evaluate the turn-on energy loss (or turn-off loss) will underestimate the actual turn-on loss in a device [8].

The energy loss in the device channel at the turn-off event is denoted as E_{off}. Then, the switching-energy loss of a device for a switching cycle is given as

$$E_{\mathrm{sw}} = E_{\mathrm{on}} + E_{\mathrm{off}}. \tag{5}$$

For WBG devices, the turn-off energy loss is significantly lower compared to turn-on loss [9], [10]. This is because the channel current of WBG devices can be cut off rapidly (due to their lower C_i) before v_{DS} starts to rise, drastically reducing any VI-overlap loss at the turn off. And therefore, in this analysis, we assume that is E_{sw} dominated by E_{on}:

$$E_{\mathrm{sw}} \approx E_{\mathrm{on}}. \tag{6}$$

Finally, the power loss in a device is given by

$$P_{\mathrm{Q}} = P_{\mathrm{con}} + P_{\mathrm{sw}}. \tag{7}$$

In (7), P_{con} is the conduction power loss, and P_{sw} is the switching power loss as given by (8).

$$P_{\mathrm{sw}} = f_{\mathrm{sw}} \cdot E_{\mathrm{sw}}. \tag{8}$$

2.2 Paralleling of Power Devices and Resulting Power Losses

Let us denote the case with a single device as *1x configuration*; then we consider the case where we connect two devices of same size (or same $R_{DS(on)}$) in parallel, which we denote as *2x configuration*. We keep all the operating parameters in the circuit the same for the two configurations. The two configurations are summarised in **Table 1**.

The 2x configuration, on the one hand, offers lower P_{con} due to reduced on-state resistance (as the load current and the duty cycle are unchanged). On the other hand, it results in an increased P_{sw} because of the increased Q_G and Q_o values. The latter phenomenon is illustrated in **Figure 5**. We understand that

- the 2x configuration has a load-independent turn-on loss component of $2\cdot E_{on\text{-}Co}$ (marked by red square on the y-axis on the right figure) because of the increased Q_o.
- the $E_{on\text{-}VI}$ component of the 2x configuration will not significantly increase as the load current is unchanged; however, due to increased Q_G and Q_o values, the *VI*-overlap time increases, resulting in a slightly higher $E_{on\text{-}VI}$ compared to the 1 x configuration.

Parameter	Single device (1x)	Effective device formed by two devices in parallel (2x)
Subjected v_{DS}	V_{dc}	V_{dc}
Load current	I_L	I_L
Switching frequency	f_{sw}	f_{sw}
duty cycle	d	d
On-state resistance	$R_{DS(on)}$	$0.5\cdot R_{DS(on)}$
Output charge	Q_o	$2\cdot Q_o$
Gate charge	Q_G	$2\cdot Q_G$

Table 1 – Comparison of characteristics and operating parameters between a single device and an effective device comprised of two devices in parallel.

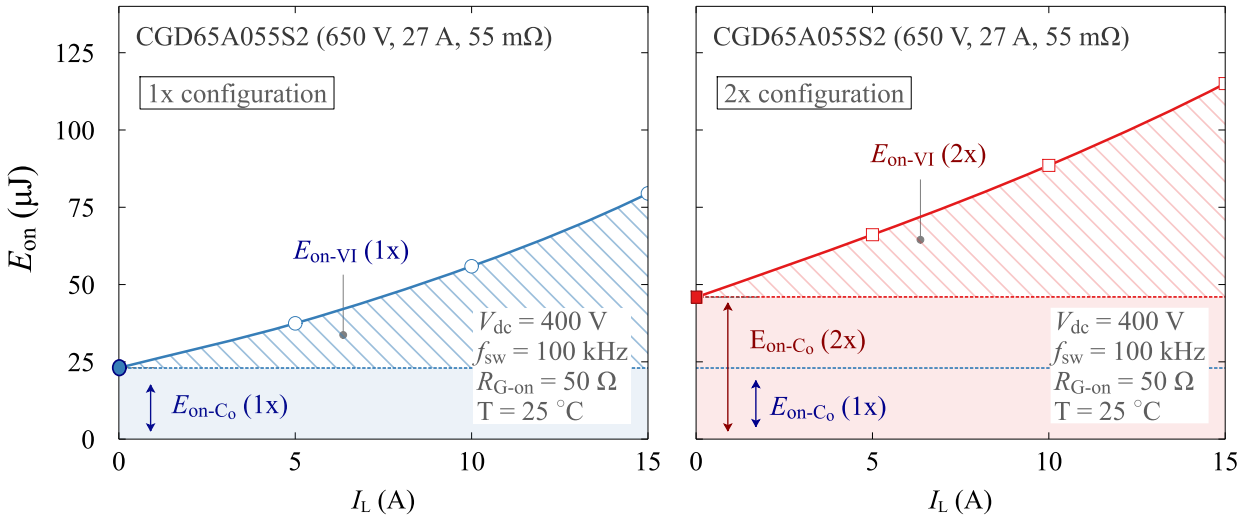


Figure 5 – Variation of turn-on energy loss (E_{on}) in device channel with load current for 1x and 2x configurations.

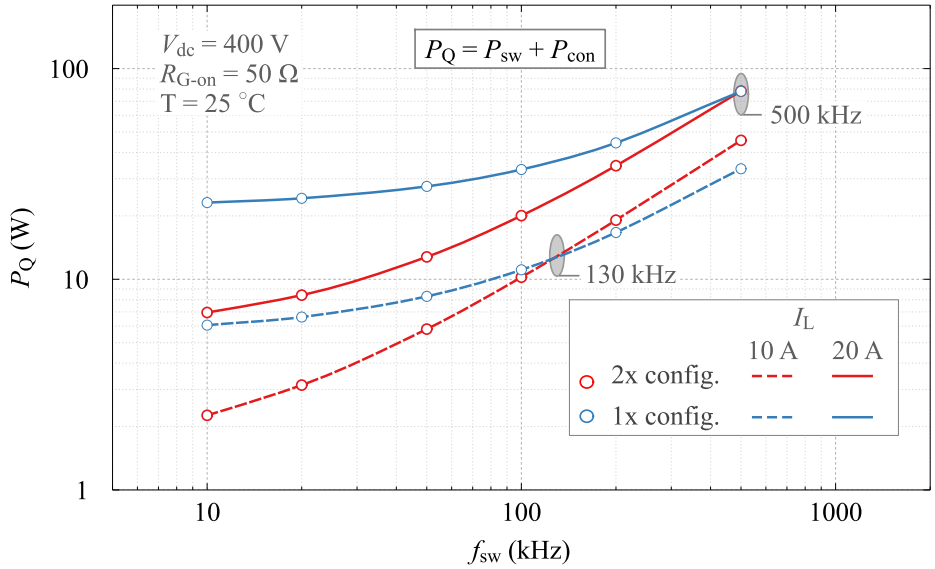


Figure 6 –Variation of total power loss (P_Q) in 1x and 2x configurations with switching frequency. Two load currents are considered.

The advantage of the 2x configuration is therefore dependent on the operation frequency as P_{sw} is a function of frequency. **Figure 6** illustrates how the total power loss changes with frequency for 1x and 2x configurations applied to the circuit in **Figure 2(a)**. A duty cycle of 0.5 is used for simplicity. Consider the case with I_L = 10 A (shown by dashed lines): the 2x configuration offers a lower P_Q at low frequencies where P_Q is dominated by conduction loss. Beyond 130 kHz, where P_Q of two configurations intersect, the 2x configuration becomes disadvantageous as the switching losses become significant enough to overcome any advantage gained by lower conduction losses. We denote this specific frequency of intersection as f_{sw}^*. Similar observations can be made for the case with I_L = 20 A (shown by solid lines). In this case, the conduction loss can dominate P_Q to a higher f_{sw}^* due to larger load current; this results in an f_{sw}^* of 500 kHz. Note that, for specific applications, correct RMS load current should be used based on the steady-state duty cycle value for the calculation of P_Q.

2.3 Gate-driver Requirements

When several devices are connected in parallel, they must be switched synchronously. Therefore, using a single gate driver will minimize any synchronization issues that may result from using individual gate drivers for each device in parallel. This requires a single gate driver to support driving of several devices and there is a practical limit to the number of devices a gate driver IC can support.

On the one hand, a gate-driving circuit is limited by the amount of average output power (P_{drive}) it can support. In bridge applications, this is limit is often imposed by the power capability of the low-voltage isolated dc-dc converters used to power the gate drivers or the maximum power dissipation capability of the gate driver IC. The power required by each power device in parallel during their turn on event is determined by the gate charge of a device, which is a parameter dependent on the size of the device.

On the other hand, a gate driver IC is limited on its peak output current at high state (known as the *source current*) and low state (known as the *sink current*). Note that for ICeGaN devices, the turn-off charge removal is facilitated by the internal miller clamp. Therefore, the sink current capability of the gate driver is unlikely to be a limitation for parallel operation of ICeGaN devices.

The effects of the two limitations described above are illustrated in **Figure 7(a)** and **Figure 7(b)**. For a given gate charge (Q_G = 6 nC is the gate charge value of a 55-mΩ CGD device) and P_{drive}, the number parallel devices that can be supported by a gate driver decreases with switching frequency– see **Figure 7(a)**. The rise time shown **Figure 7(b)** considers how much time it takes for the gate driver to charge Q_G during device's turn on event. This is achieved by the gate driver providing a peak current for a short period of time; this is known as the source current capability of the gate driver, denoted as I_{source} in **Figure 7(b)**. For example, for a rise time of 5 ns, I_{source} greater than 2 A is required to support 2 devices in parallel: the figure shows that a driver with I_{source} = 4 A can support this and handle up to 3 devices in parallel.

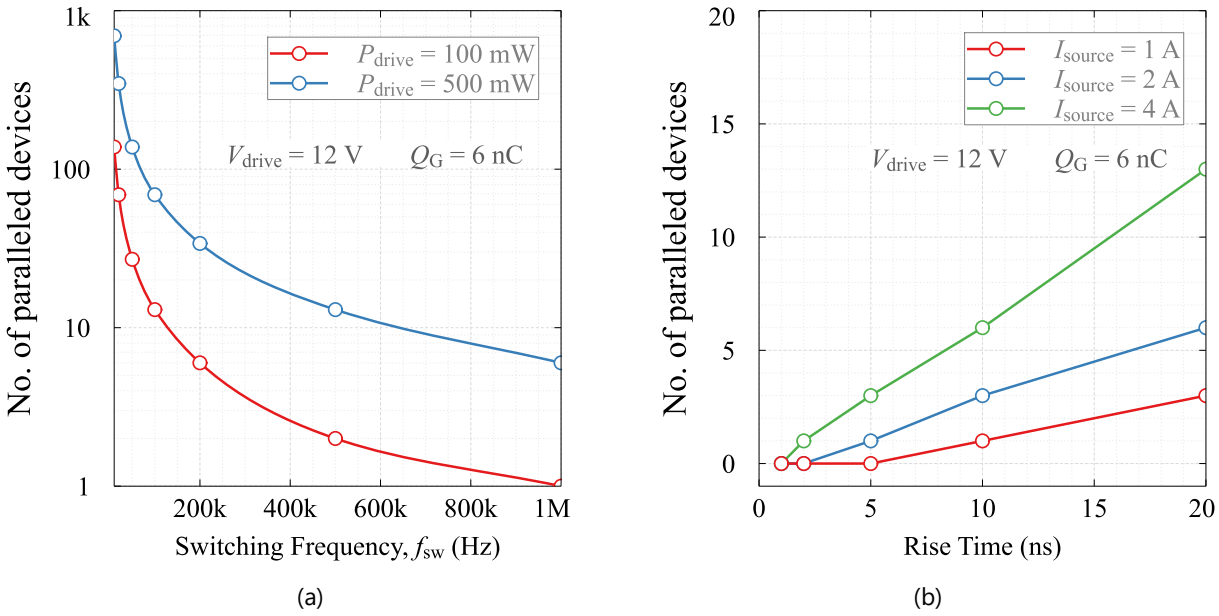


Figure 7 – Dependence of parallel operation on gate-driving capability. (a) Variation of maximum number of paralleled devices versus switching frequency for different P_{drive} values. (b) Variation of maximum number of paralleled devices versus gate voltage rise time for different I_{source} values. P_{drive} is the available gate driving power for a given low- or high-side switch; I_{source} is the peak source current capability of the gate driver in high-state output.

2.4 Important Device Aspects to Consider When Paralleling

The considerations presented **Subsections 2.2** and **2.3** are basic requirements that should be satisfied for parallel operation from a design perspective. Then, from a power device perspective, there are several factors that should be taken into consideration for proper implementation of a parallel solution, which is the focus of this subsection.

2.4.1 Manufacturing Spread

The most difficult consideration in connecting devices in parallel is the manufacturing spread (device–device parameter variations, or simply device mismatches) among the chosen devices. This is determined by the *manufacturing process capability*, which is highly dependent on the actual fabrication processes used by a power semiconductor manufacturer and the repeatability of the process output. In terms of parallel operation, device–device variation of the following parameters should be understood.

1. $R_{DS(on)}$
2. $V_{GS(th)}$
3. Q_G (or gate input capacitance C_i)

In practice, a power supply designer would prefer tight tolerance in these parameters.

2.4.2 Static versus Dynamic Current Sharing

When two or more devices are connected in parallel, ideally, we want the devices to share the load current equally among them. However, due to mismatches in the device parameters, this is not practically tenable. And the effect of device mismatches can be explained by looking at two distinct aspects as shown in **Figure 8**:

1. static operation
2. dynamic operation

Here, in the **Figure 8** we have considered the 1x configuration (Q_1 bottom device and Q2 top device in half-bridge arrangement) to clarify the terms. Static operation considers the conduction period (when turn-on and turn-off transitions are fully completed) of a device, whereas dynamic operation accounts for the switching transitions.

With the above definition, in parallel configurations, *static current sharing* considers the sharing of load current among devices during conduction period. A mismatch in $R_{DS(on)}$ among the devices will result in unequal currents among the devices during conduction. *Dynamic sharing* entails sharing among paralleled devices during switching events, and it is mainly affected by mismatches in $V_{GS(th)}$ and Q_G. Such mismatches would result in unequal E_{on} and E_{off} values and peak channel current during switching events.

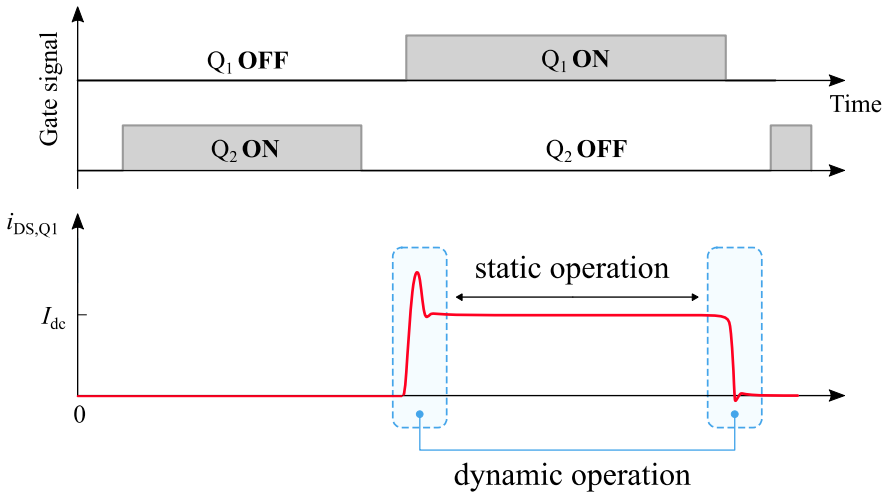


Figure 8 – Static and dynamic operation periods during a general switching cycle.

ICeGaN Parameter	Temperature dependence
$R_{DS(on)}$	PTC
$V_{GS(th)}$	Small NTC
Q_G	No dependence

Table 2 – Temperature dependence of ICeGaN parameters

A detailed discussion on device parameters and their effect on parallel operation will be presented in **Section 3**.

2.4.3 Temperature Dependence of Device Parameters

Any temperature dependence of the parameters introduced **Section 2.4.1** will also affect the current sharing in parallel operation. These can be summarised as follows.

- $R_{DS(on)}$ is temperature dependent and has a positive temperature coefficient (PTC) for Si MOSFETs and e-GaN HEMTs such as ICeGaN™ [11]. SiC devices, on the other hand, show a negative temperature coefficient (NTC) at low temperatures and a PTC at high temperatures [12], [13].
- $V_{GS(th)}$ has a smaller NTC for e-GaN HEMTs compared to a Si MOSFETs [14], [15].
- Q_G is a temperature independent parameter for power FETs [16].

A summary of temperature dependence of ICeGaN parameters are given in **Table 2**. Temperature dependence of $R_{DS(on)}$ and $V_{GS(th)}$ and their effect on parallel operation will be detailed in **Section 3**.

2.4.4 Peak Current

In general, when devices are selected for parallel operation, it is important to make sure that peak current through each device during switching events is within device's pulsed current capability [4]. And this should still be satisfied under worst-case parameter mismatches where devices carry different peak channel currents.

2.5 Circuit Parasitics

Circuit parasitics are practically unavoidable in power converter designs. For parallel operation, it is mainly the parasitics present in the PCB that could create undesirable behaviour. For example, if the parasitic inductances present in the turn-on gate path to two devices connected in parallel are not equal, it could result in a considerable time delay between the turn-on events of the two devices. Therefore, it is extremely important the circuit layout is kept symmetric. Although this application note does not go into detail on symmetrical PCB layout guidelines, **Section 3.2** highlights effects of circuit parasitics and how they impact dynamic current sharing.

2.6 Thermal Aspects to Consider When Paralleling Power Devices

Power dissipation in each device should also be considered in the design stage when a parallel configuration is sought. This subsection introduces basic concepts in relation to this; a practical example is considered in **Section 3.1**.

2.6.1 Simplified Thermal Circuits

Figure 9(a) shows a simplified thermal circuit of a power device: the total power dissipated (P_Q) in device is modelled as current source. The junction to case and case to ambient thermal resistances are modelled by the resistances $R_{\theta Q,J\text{-}C}$ and $R_{\theta Q,C\text{-}A}$, respectively. **Figure 9(b)** provides a detailed view on the junction to case thermal impedance, according to the *Cauer* thermal model, where the time behaviour is modelled by the network of capacitors. The simulation results that are presented in **Section 3.1** are carried out using the Cauer model.

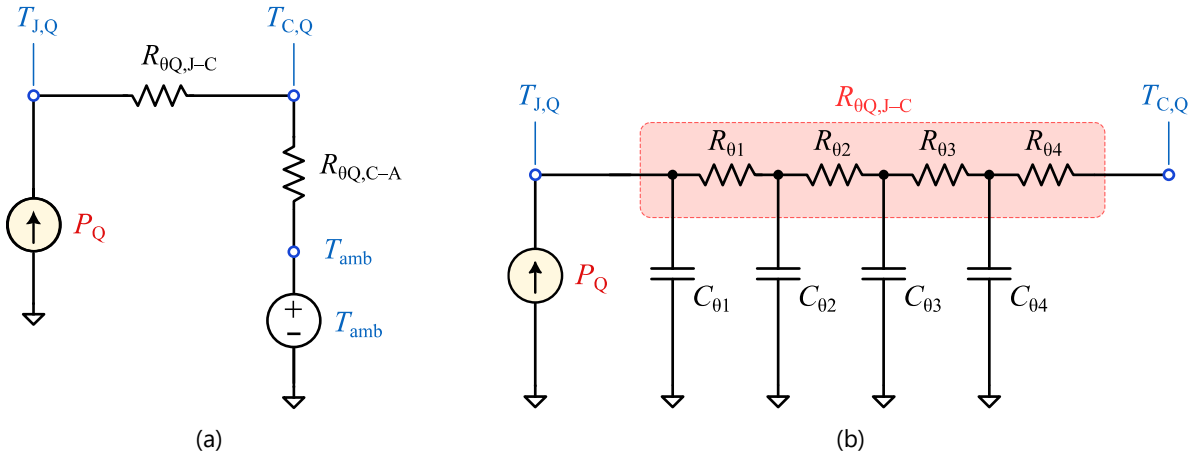


Figure 9 – (a) Thermal circuit for a single device (b) Cauer Model detailing the junction to case thermal impedance.

2.6.2 Importance of Thermal Cross Coupling

Apart from the possibility of exceeding channel current, the main undesirable outcome of device mismatches on parallel operation is the unequal power dissipation, and hence unequal junction temperatures, in devices connected in parallel. This could either be caused by a mismatch in $R_{DS(on)}$ or/and $V_{GS(th)}$. If not addressed during the design stage, unequal power dissipation could lead to excessive junction temperatures in a particular device and cause a failure in the power converter [17]. This can be alleviated by having a tight thermal coupling between the devices in parallel (this is verified in **Section 3**).

Figure 10 shows the simplified thermal circuit for two devices connected in parallel on printed circuit board (PCB). In experimental work presented in **Section 3**, we have used bottom-side-cooled devices. Consequently, the thermal cross coupling between the two devices is mainly along the PCB, which is denoted by a thermal resistance $R_{\theta,QA-QB}$. For tight thermal cross coupling, $R_{\theta,QA-QB}$ should be reduced as much as possible during the PCB layout design stage.

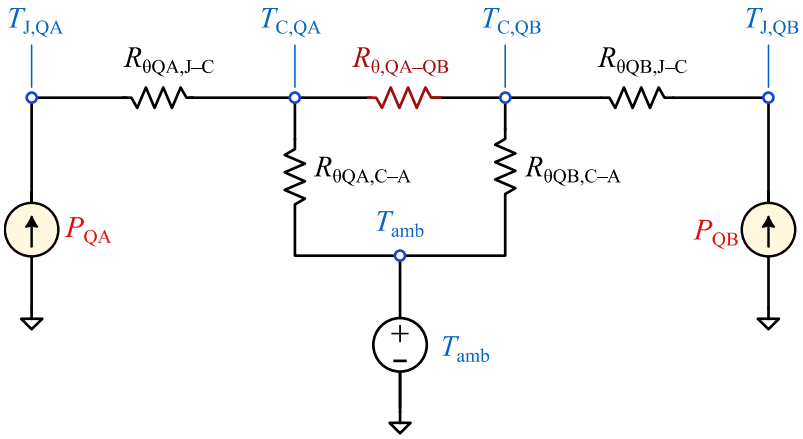


Figure 10 – Simplified thermal circuit for two devices (Q_A and Q_B) in parallel placed on a printed circuit board.

3 Parallel Operation of Power Devices in Practice

This section presents parallel operation of power GaN HEMTs in practice using both simulation and experimental results.

Notes:

- For all the analysis and results presented in this section we use two CGD65A055S2 ICeGaN devices (55 mΩ and 650 V). For simulations, version 0.4 of CGD65A055S2 SPICE model is used.
- The two devices are connected in parallel on the high side (denoted as Q_A and Q_B) and act as the devices under test.

3.1 Static Current Sharing

When two devices are connected in parallel, the sharing of the load current in static operation is affected by two mechanisms.

1. Self-balancing of currents due to PTC of $R_{DS(on)}$ of e-GaN HEMTs.
   The device with lower $R_{DS(on)}$ will carry a larger current. This is because, the device with lower $R_{DS(on)}$ will dissipate more power due to larger current it carries, increasing its junction temperature; this increases its $R_{DS(on)}$, ultimately lowering its current [17]. In parallel configuration, this mechanism is better supported by lower thermal cross coupling between the devices [18].
2. Thermal cross coupling between the devices.
   This acts on to equalize the junction temperature of the two devices. As emphasized in **Section 2.6.2**, tight thermal cross coupling results in lower overall junction temperatures [18]. This is verified with the results in this section.

The test circuit shown in **Figure 11** is used to observe static current sharing between two devices connected in parallel. The current through each device is measured using sense resistors (R_{senseA} and R_{senseB}). The steady-state dc load current is controlled by choosing an appropriate value for R_{load}. First the two devices are turned on with zero dc-link voltage and then at t = 0, V_{dc} is applied.

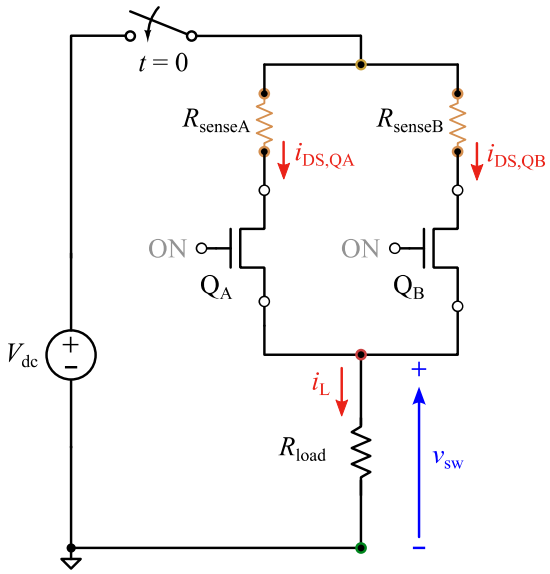


Figure 11 – Test circuit used to investigate 'static' current sharing.

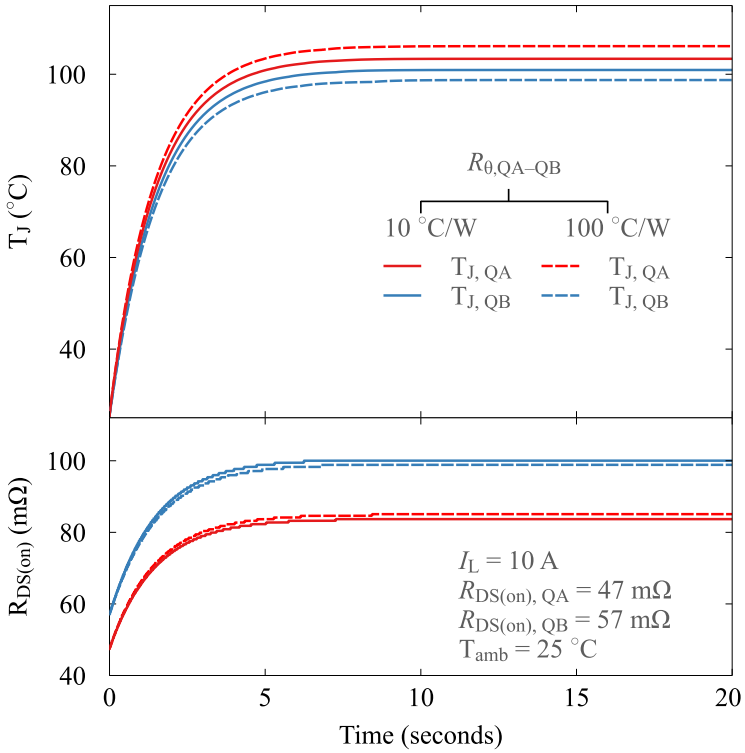


Figure 12 – Simulation results showing the effect of different $R_{\theta,QA–QB}$ (or thermal cross coupling) values on T_J. Conditions: $R_{\theta Q,J\text{-}C}$ = 1.3 °C/W; $R_{\theta Q,C\text{-}A}$ = 30 °C/W; T_{amb} = 25 °C; V_{dc} = 63 V; R_{load} = 6 Ω.

First, to showcase the effect of $R_{DS(on)}$ mismatch and tight cross-coupling on parallel operation, we have implemented the test circuit on a SPICE simulation platform, where $R_{DS(on),QA}$ = 47 mΩ and $R_{DS(on),QB}$ = 57 mΩ. $R_{\theta Q,J\text{-}C}$ and $R_{\theta Q,C\text{-}A}$ values are taken as 1.3 °C/W and 30 °C/W, respectively. The results are presented in **Figure 12**. We have considered two $R_{\theta,QA–QB}$ values: 10 °C/W indicated by solid lines and 100 °C/W indicated by dashed lines. Although having a lower $R_{\theta,QA–QB}$ value increases $\Delta R_{DS(on)}$ between the two devices (solid lines in the bottom figure in **Figure 12**), it creates a considerable reduction in ΔT_J between the two devices (solid lines in the top figure in **Figure 12**). This signifies that having tight thermal coupling between paralleled devices helps to balance the junction temperatures among them, especially when they have mismatched $R_{DS(on)}$ values.

Figure 13 shows experimental results for T_C and ΔT_C variation with time for two devices connected in parallel with different $R_{DS(on)}$ values (49.8 mΩ and 53.7 mΩ). First, ΔT_C start to increase due to the difference in $R_{DS(on)}$ between the two devices; however, this value stabilizes to a fixed value of 3 °C after about 3 minutes, although the absolute case temperatures are still increasing. This is mainly due to tight thermal cross coupling between the two devices. After 20 minutes the case temperatures also stabilize, while ΔT_C remains unchanged.

The current waveforms (in relation to the above experiment) are plotted in **Figure 14** in a much smaller time scale. It can be observed that the load current is shared well between the two devices without significant differences. Device Q_A carries a slightly higher current as expected due to its lower $R_{DS(on)}$.

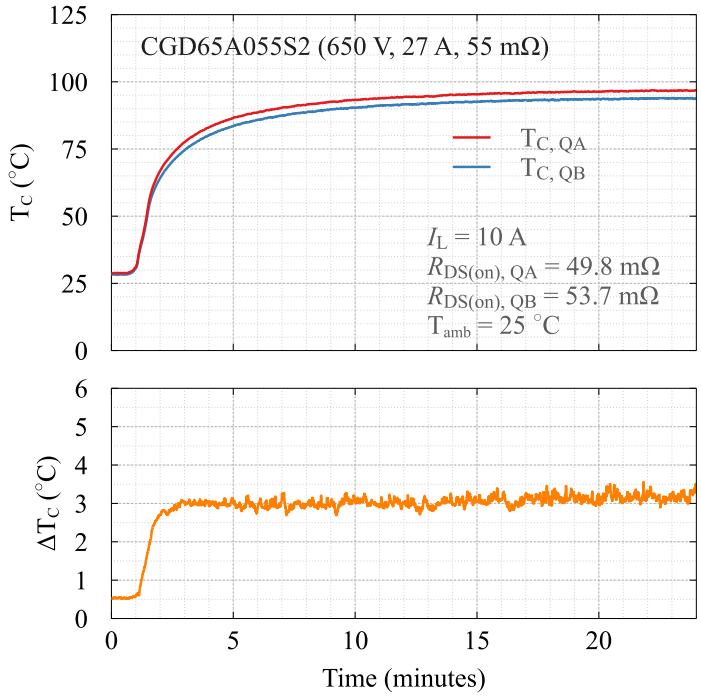


Figure 13 – Experimental results showing the variation T_C and ΔT_C with time in static current sharing. Conditions: T_{amb} = 25 °C; V_{dc} = 63 V; R_{load} = 6 Ω.

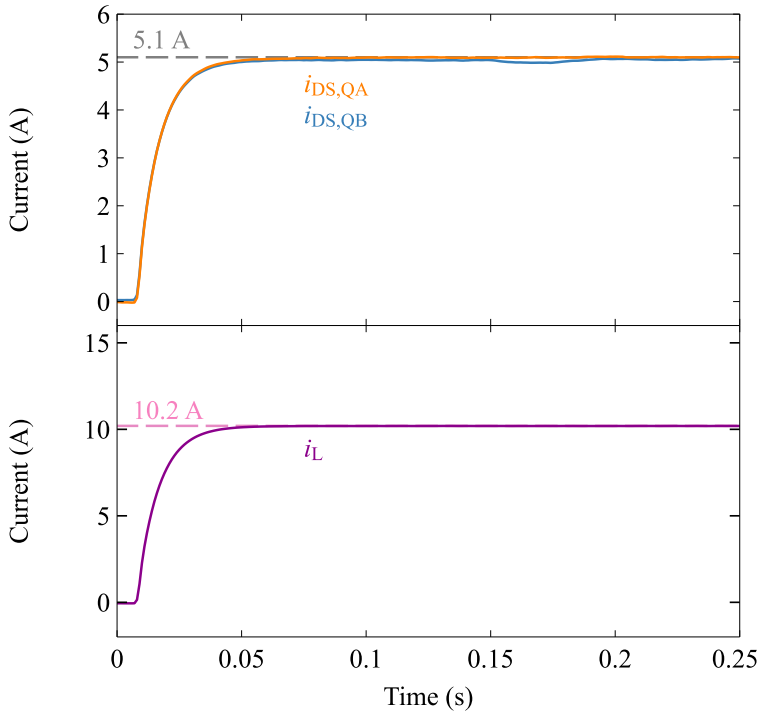


Figure 14 – Experimental current waveforms at start-up. Conditions: T_{amb} = 25 °C; V_{dc} = 63 V; R_{load} = 6 Ω.

3.2 Dynamic Current Sharing

In this subsection effects of mismatches $V_{GS(th)}$ and Q_G on dynamic current sharing is investigated with both simulation and experimental results. The test circuit used to investigate dynamic current sharing is given in **Figure 15**. The arrangement is quite similar to the setup used in **Section 3.1**. However, in this case the devices are switched in the following manner: 1) first, keep the devices off; 2) then apply the dc-link voltage; 3) finally, turn both devices are turned on and off for several pulses. We have employed asymmetrical gate driving with separate turn-on and turn-off gate resistances. External circuit parasitics in the test circuit can be represented as bulk inductive and capacitive components as shown in **Figure 16**.

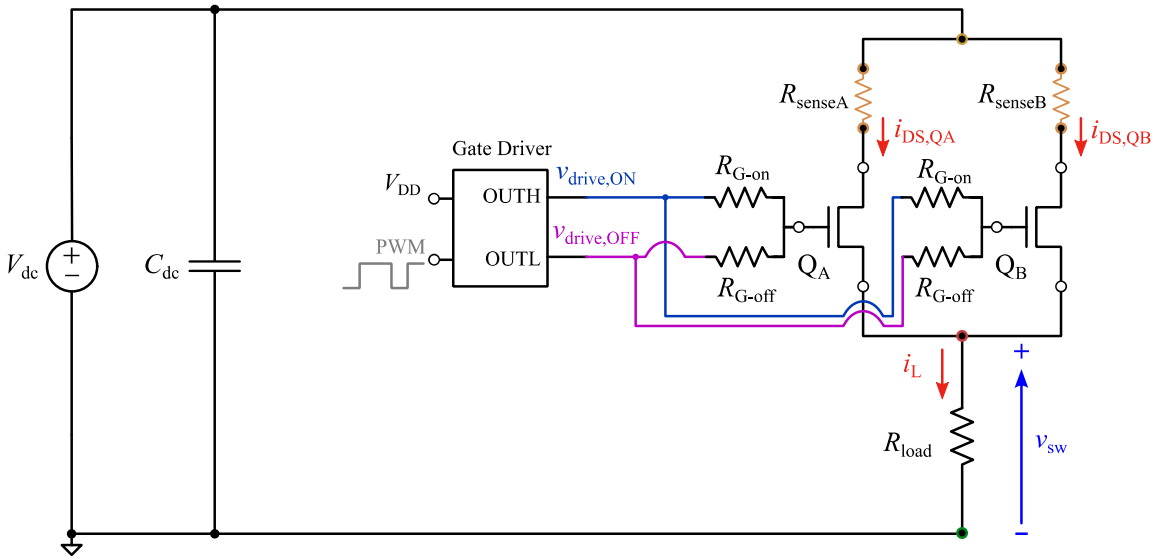


Figure 15 – Test circuit used to investigate 'dynamic' current sharing (no parasitics shown).

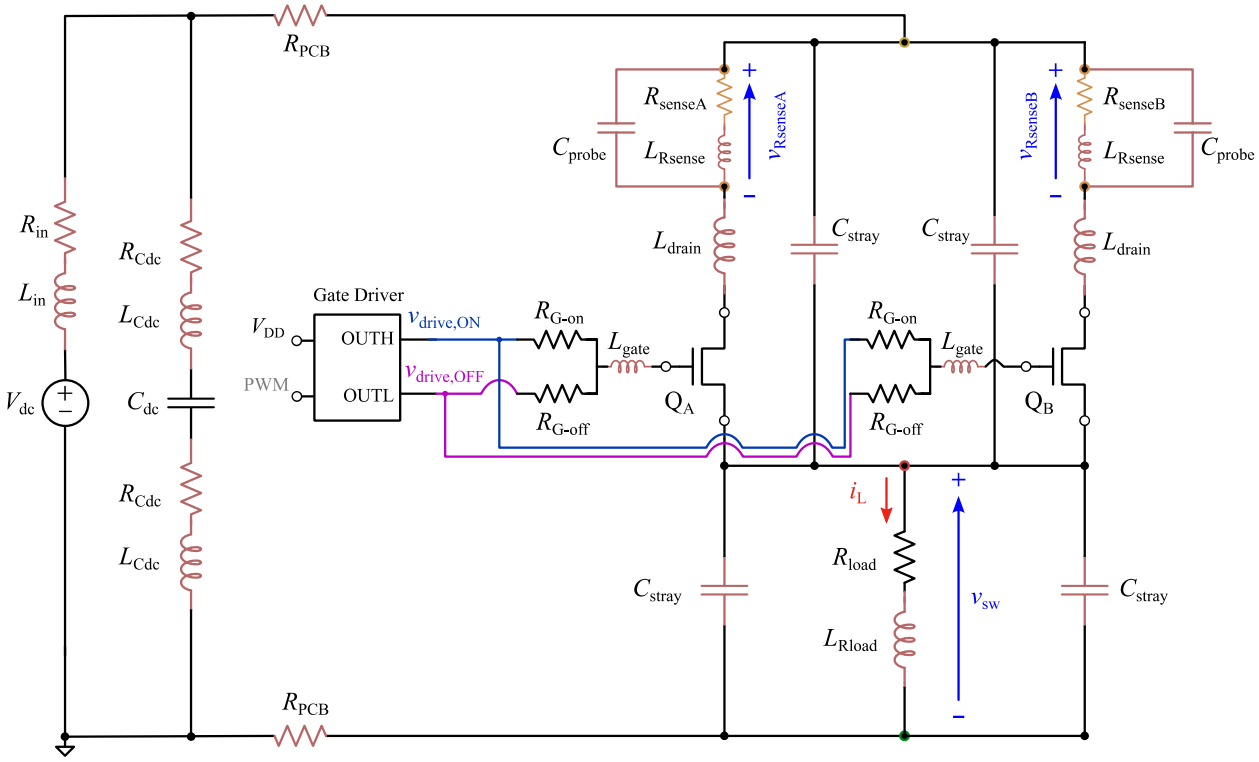


Figure 16 – Test circuit used to investigate 'dynamic' current sharing (parasitics shown in light brown).

Note that parasitics are applied symmetrically to the simulation model. It should be emphasized that drain currents ($i_{DS,QA}$ and $i_{DS,QB}$) are calculated using the voltage measured across the sense resistors ($v_{RsenseA}$ and $v_{RsenseB}$) to recreate the experimental conditions:

$$i_{\mathrm{DS,QA}} = \frac{v_{\mathrm{RsenseA}}}{R_{\mathrm{senseA}}} \tag{9}$$

$$i_{\mathrm{DS,QB}} = \frac{v_{\mathrm{RsenseB}}}{R_{\mathrm{senseB}}} \tag{10}$$

Any inductance between the two measurement points will create considerable ringing in the observed voltage. **Figure 17** and **Figure 18** aim to provide some context to the effect of parasitics on the dynamics and observation of voltage and currents in the circuit, when there is no mismatch between device parameters (in other words Q_A and Q_B are identical).

For the turn-on event (see **Figure 17**), drain currents exhibit considerable ringing; this is mainly due to parasitic inductances in drain current path (between dc-link and the power device) as well across the sense resistors (see **Figure 16**).

For the turn-off event (see **Figure 18**), parasitics also introduce appreciable ringing to drain currents. For both turn-on and turn-off, the effect of parasitics on the gate voltages are not appreciable. Note that for simulation results in this section, we have shown the *internal* gate voltage of ICeGaN devices [5], i.e., the gate–source voltage of the internal power HEMT of ICeGaN devices.

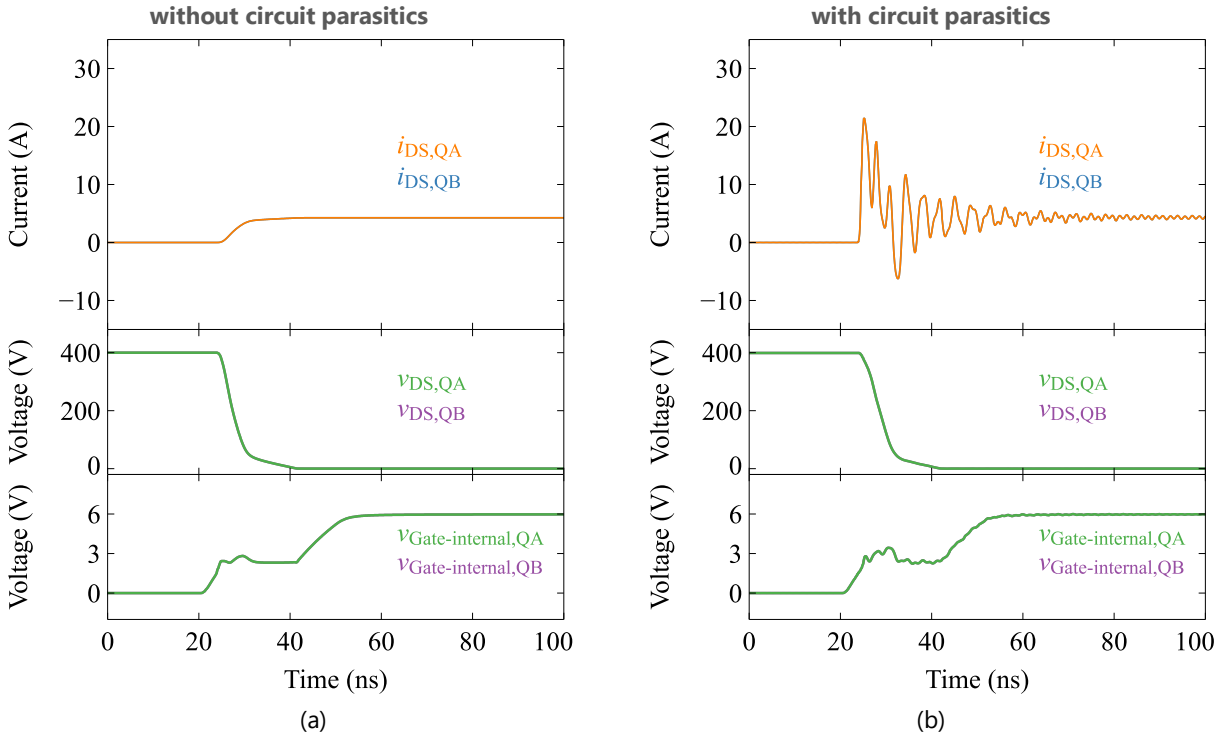


Figure 17 – Simulation results comparing the turn-on event dynamics (a) without circuit parasitics and (b) with circuit parasitics. Conditions: identical Q_A and Q_B; V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω.

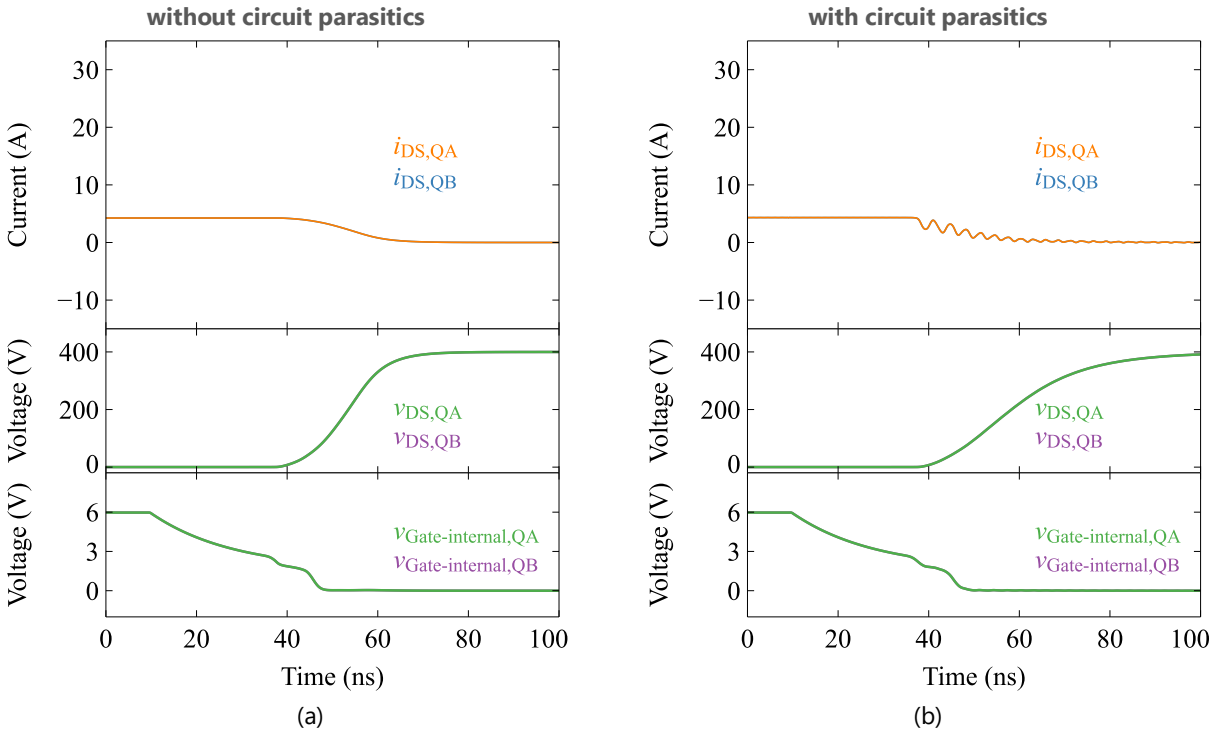


Figure 18 – Simulation results comparing the turn-off event dynamics (a) without circuit parasitics and (b) with circuit parasitics. Conditions: identical Q_A and Q_B; V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω.

3.2.1 $V_{GS(th)}$ Mismatch

For device threshold voltage, a power supply designer would ideally like tight tolerance between device samples.

Consider two devices (Q_A and Q_B) in parallel operation where they are driven by a single gate driver with identical gate driving paths and resistances. The two devices have same Q_G values, but they differ in $V_{GS(th)}$ such that $V_{GS(th),QB} > V_{GS(th),QA}$. In this case, Q_A will turn on before Q_B when the gate driver applies a high-state signal as illustrated in **Figure 19**. However, at the turn off, Q_B will turn off before Q_A as the decreasing gate voltage approaches $V_{GS(th),QB}$ first.

The implication of the above situation is first considered in a simulation-based analysis with a 0%, 10%, and 20% mismatch of $V_{GS(th)}$ between Q_A and Q_B. A dc-link voltage of 400 V and a load current of 8 A is used. For this simulation, circuit parasitics are ignored. The results are tabulated in **Table 3**, and the following observations can be made:

- the peak channel current[1] sharing is 56% and 42% between the two devices.
- turn-on energy loss sharing is 61% to 39% between the two devices.

According to **Table 3**, total turn on energy loss is not affected by the mismatches. This can be understood as follows in relation to hard switching.

1. The $E_{on\text{-}Co}$ component depends only on Q_o value of the devices, and therefore, is independent on $V_{GS(th)}$.
2. The E_{on}-VI component depends on the external load current through each device and the voltage fall time of device v_{DS}. When two devices are considered collectively, $V_{GS(th)}$ mismatch does not change either total load current or voltage fall time.

[1] We have specifically considered the channel current through the device as this is the actual current through the device. However, in experimental measurements, only the drain currents can be measured.

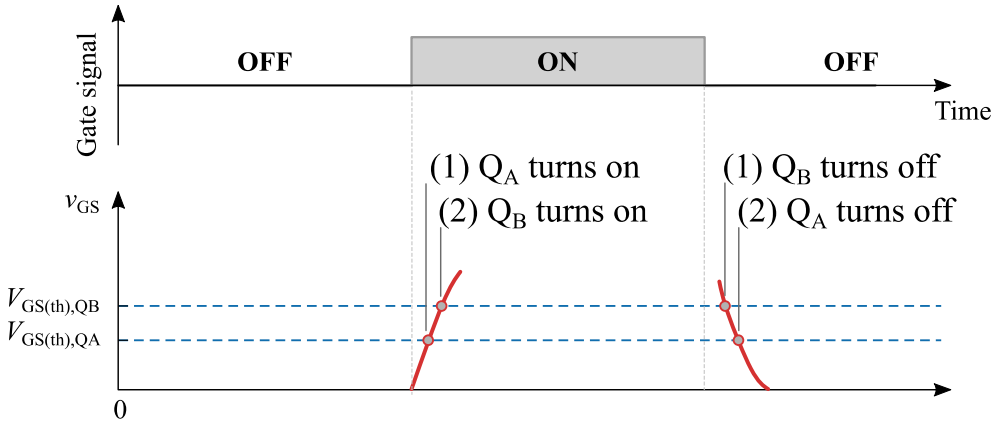


Figure 19 – Turn-on and turn-off event distribution between two devices Q_A and Q_B operating in parallel when $V_{GS(th),QB} > V_{GS(th),QA}$ and the two devices have identical Q_G values.

Test Case	$V_{GS(th)}$ Variation	Sharing of $I_{CH(peak)}$		Total E_{on} (µJ)	Sharing of E_{on}	
		Q_A	Q_B		Q_A	Q_B
1	0%	50.0%	50.0%	18.9	50.0%	50.0%
2	10%	52.9%	47.1%	19.0	55.5%	44.5%
3	20%	55.8%	44.2%	19.1	60.9%	39.1%

Table 3 – Simulation results showing dynamic current sharing between the two devices Q_A and Q_B at turn on under $V_{GS(th)}$ mismatches. Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω; circuit parasitics ignored.

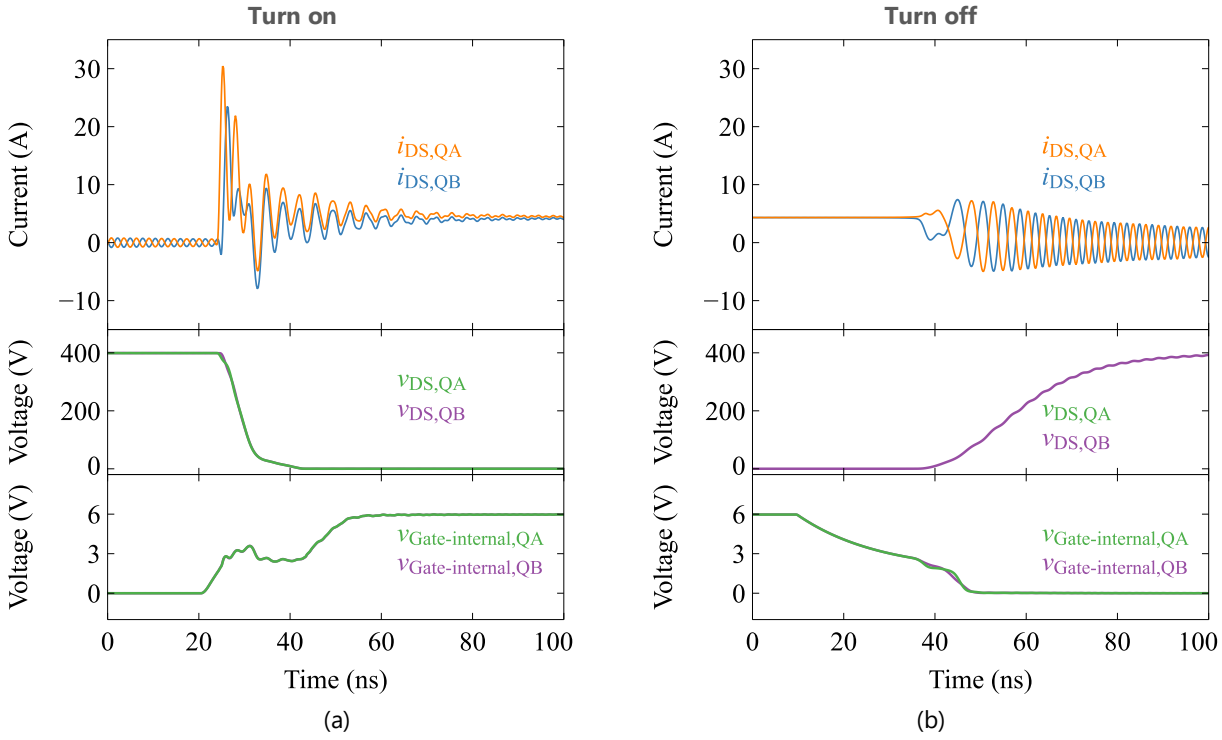


Figure 20 – Simulation results showing the effect of $V_{GS(th)}$ mismatch considering circuit parasitics. Device details: $V_{GS(th),QB} > V_{GS(th),QA}$ with 20 % mismatch. Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω.

Figure 20 shows waveforms based on simulation results for a 20% mismatch of $V_{GS(th)}$ with $V_{GS(th),QB} > V_{GS(th),QA}$. In this case, we have considered circuit parasitics to provide a fair comparison with the experimental observations that follow. At the

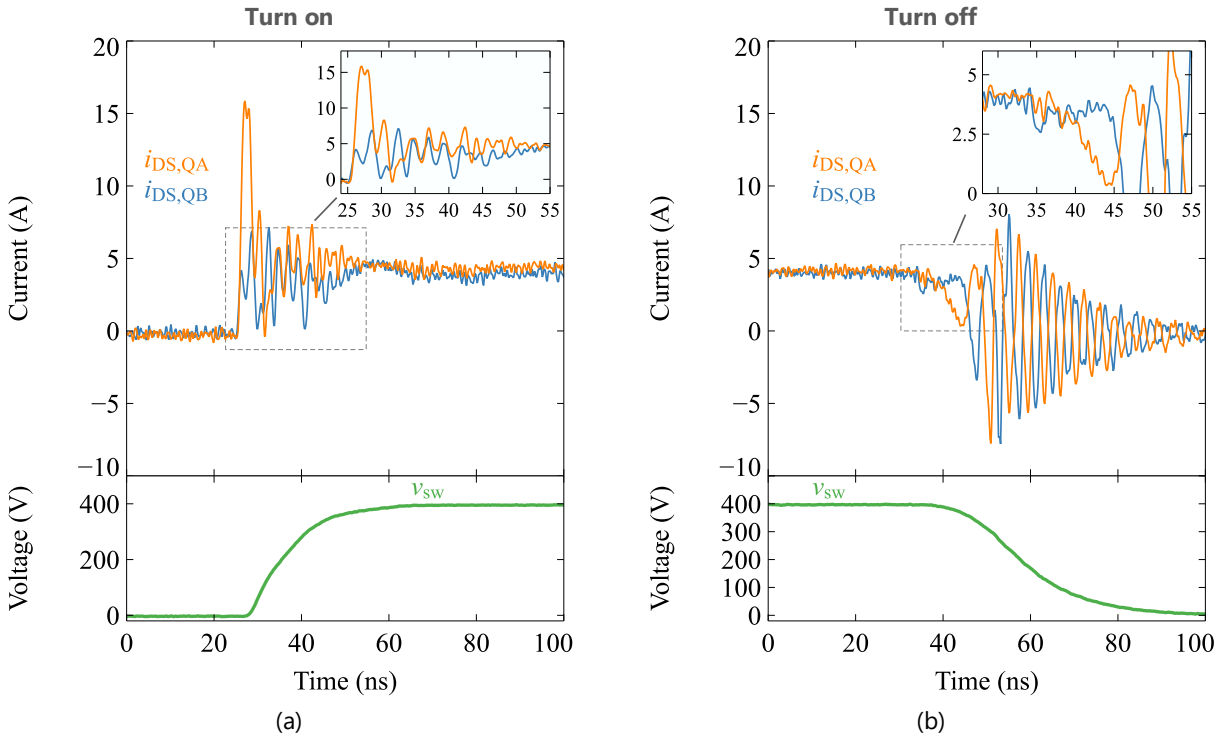


Figure 21 – Experimental results showing the effect of $V_{GS(th)}$ mismatch. Device details: $V_{GS(th),QA}$ = 2.75 V and $V_{GS(th),QB}$ = 3.08 V (with 11% mismatch). Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω.

turn on, the drain current of Q_A starts to flow first as expected and caries a much larger peak current than Q_B. Both devices experience the same v_{DS} as was explained previously. Then, at the turn-off event Q_B switch off first (its channel gets cuts off) and its drain current starts to fall first. This is followed by the switch-off of Q_A; the subsequent ringing in the two drain currents is due to the unbalanced parasitics in the circuit.

Experimental waveforms for a case with $V_{GS(th),QB} > V_{GS(th),QA}$ (with 11% mismatch) are plotted in **Figure 21**. Similar to the simulation results in **Figure 20**, Q_A switches on before Q_B. The interpretation of the turn-off transient is challenging due to the measurement noise; however, the zoomed inset on the turn-off transient shows Q_B current starting to fall first around 35 ns.

3.2.2 Effect of the NTC of $V_{GS(th)}$

For $V_{GS(th)}$, ideally, a designer would prefer a zero-temperature coefficient, or a positive one. When there is a mismatch among the $V_{GS(th)}$ value of paralleled devices, an NTC will further decrease $V_{GS(th)}$ of the device with the lowest $V_{GS(th)}$. This seems a potential disadvantage leading to increased E_{on} on the device with the lowest $V_{GS(th)}$ at elevated temperatures. However, it should also be understood that $V_{GS(th)}$ of the rest of the parallel devices would also decrease. The final effect of this can be understood as follows.

Table 4 tabulates how the $V_{GS(th)}$ spread of 55-mΩ CGD devices vary with temperature (experimental); peak current sharing and E_{on} sharing details are also tabulated (simulation based). The table highlights that the $V_{GS(th)}$ spread stays between 20% to 40% through the whole temperature range. It can be observed that the effect of such variation is minimal: sharing of channel current remains stable around 55:45% and sharing of E_{on} is fixed around 60:40%. Total E_{on} increases by 4.8% at 110 °C (compared to 25 °C), and 14% increase at 150 °C (compared to 25 °C). These increases are mainly due to the increased turn on time at high temperatures.

Test Case	Temperature (°C)	$V_{GS(th)}$ Variation	Sharing of $I_{CH(peak)}$		Total E_{on} (µJ)	Sharing of E_{on}	
			Q_A	Q_B		Q_A	Q_B
1	-55	21%	55.5%	44.5%	18.3	60.5%	39.5%
2	25	31%	57.1%	42.9%	18.9	63.4%	36.6%
3	110	29%	55.3%	44.8%	19.8	60.1%	39.9%
4	150	39%	56.1%	43.9%	21.2	62.6%	37.4%

Table 4 – Simulation results showing the effect of the NTC $V_{GS(th)}$ on dynamic current sharing between the two devices Q_A and Q_B at turn on. Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω; circuit parasitics ignored.

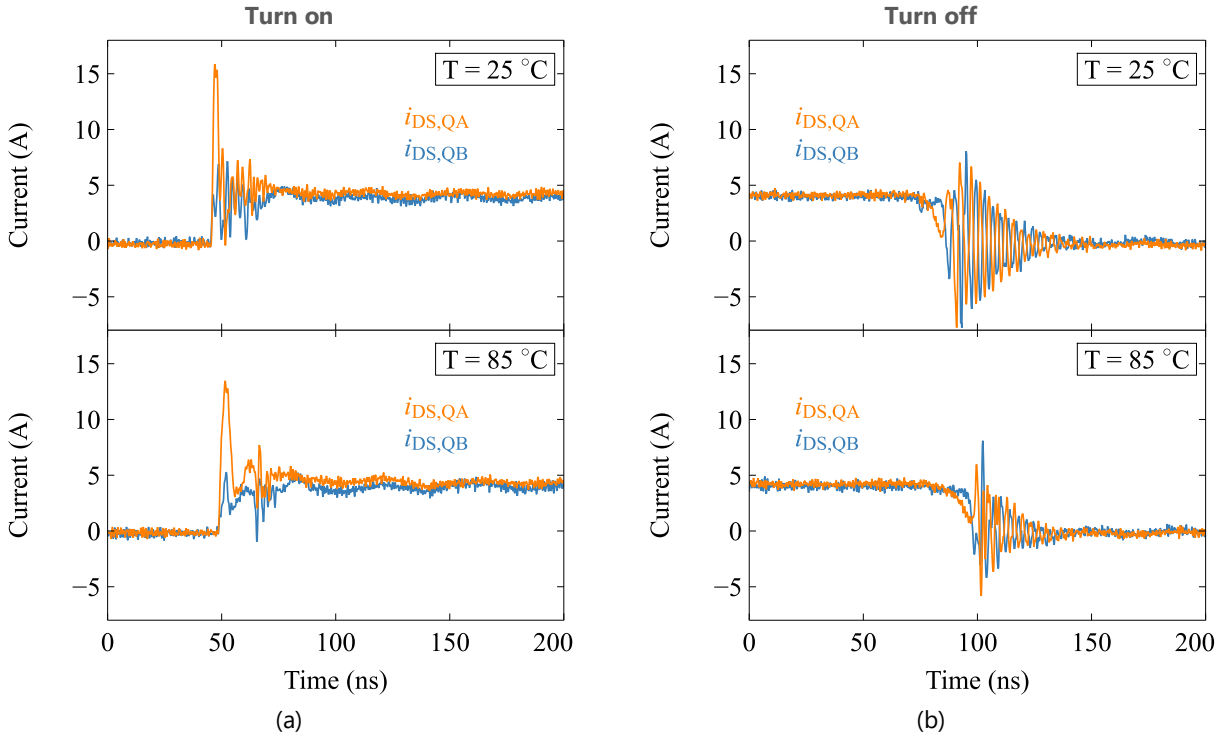


Figure 22 – Experimental results showing the effect NTC of $V_{GS(th)}$. Device details: $V_{GS(th),QA}$ = 2.75 V and $V_{GS(th),QB}$ = 3.08 V at 25 °C. Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω.

Figure 22 plots turn-on and turn-off drain current waveforms for two devices connected in parallel (same devices used in **Figure 21**) at 25 °C and 85 °C case temperatures. The results suggest no deterioration in current sharing at 85 °C supported by good thermal coupling between the two devices. The reduction in ringing at elevated temperature is due to the increased damping introduced by increased $R_{DS(on)}$ of the devices.

There is another effect of mismatched $V_{GS(th)}$; it increases overall on time of the device with lower $V_{GS(th)}$ (see **Figure 19**). However, considering the timescale of this increment, we assume that the increased conduction loss that device is negligible in contrast to the increment in E_{on}.

3.2.3 Q_G Mismatch and Countermeasures

The simplified diagram in **Figure 23** illustrates turn-on and turn-off events when two paralleled devices have mismatched Q_G such that $Q_{G,QA} > Q_{G,QB}$ (or equivalently, Q_A has higher input capacitance compared to Q_B). As charging of Q_B takes less time due to its lower input capacitance, Q_B will turn on before Q_A, when the gate driver applies a high-state signal. At the turn off, Q_B will still turn off first as it input capacitance gets discharged faster compared to that of Q_A.

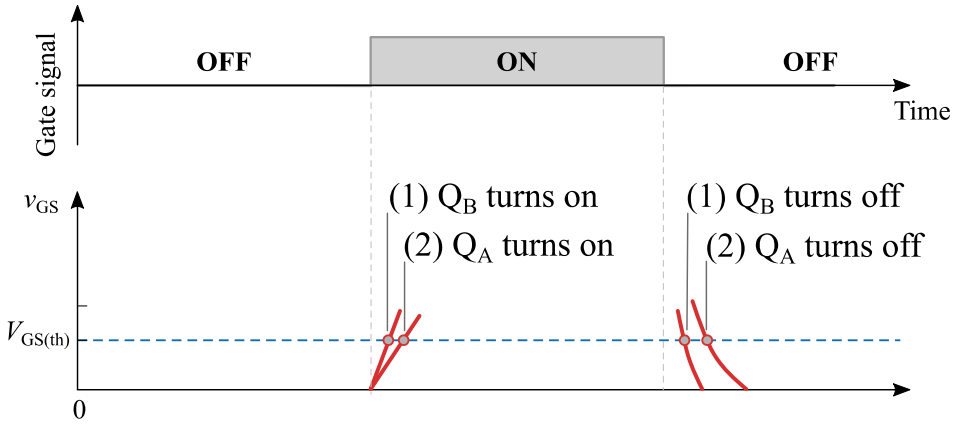


Figure 23 – Turn-on and turn-off event distribution between two devices Q_A and Q_B operating in parallel when $Q_{G,QA} > Q_{G,QB}$ and the two devices have identical $V_{GS(th)}$ values.

Test Case	C_{GS} Variation	Sharing of $I_{CH(peak)}$		Total E_{on} (µJ)	Sharing of E_{on}	
		Q_A	Q_B		Q_A	Q_B
1	0%	50.0%	50.0%	18.9	50.0%	50.0%
2	10%	47.2%	52.8%	19.0	45.6%	54.4%
3	20%	44.6%	55.4%	19.0	41.4%	58.6%

Table 5 – Simulation results showing dynamic current sharing between the two devices Q_A and Q_B at turn on under C_{GS} mismatches ($C_{GS,QA} > C_{GS,QB}$). Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω; circuit parasitics ignored.

An example on the impact of mismatched Q_G on parallel operation is given by the simulation results in **Table 5**. It considers 0, 10, and 20 percent mismatches of C_{GS} for CGD 55-mΩ devices.[2] The following observations can be made:

- The peak channel current sharing is 55.4% and 44.6% between the two devices.
- Turn-on energy loss sharing is 58.6% to 41.4% between the two devices.
- Total E_{on} stays fixed independent of the mismatch due to reason explained in **Section 3.2.1**.

Figure 24 plots waveforms based on simulations for $C_{GS,QA} > C_{GS,QB}$ (or equivalently $Q_{G,QA} > Q_{G,QB}$) considering circuit parasitics. At the turn-on event, Q_B switches on first, then followed by Q_A. At the turn-off, Q_B turn-off first. As the current in Q_B starts to decrease, the drain current of Q_A increases in order to support the load current; this trend halts as soon as Q_B goes through its turn-off. **Figure 25** shows an experimental example of Q_G mismatch with $Q_{G,QA} > Q_{G,QB}$: a good correlation between simulation and experimental results can be observed.

Having either an increased $R_{G\text{-}on}$ value or C_i (or equivalently Q_G) effectively results in an increased RC value for the charging process of device gate with respect to its source. To counter any mismatches in Q_G (or the RC value in general) corresponding to each device in parallel, a common gate resistance (R_{GC}) can be put in between the gate driver output and the individual gate resistors going into the gates of each device–see **Figure 26**. We only consider the turn-on event in our analysis as the turn off is achieved by the internal miller clamp for ICeGaN devices.

[2]We have considered C_{GS} as the mismatched parameter here in the simulations here as it Q_G cannot be altered in a direct manner. We have also assumed negligible contribution from C_{DG} on Q_G, i.e., $C_{GS} \gg C_{DG}$.

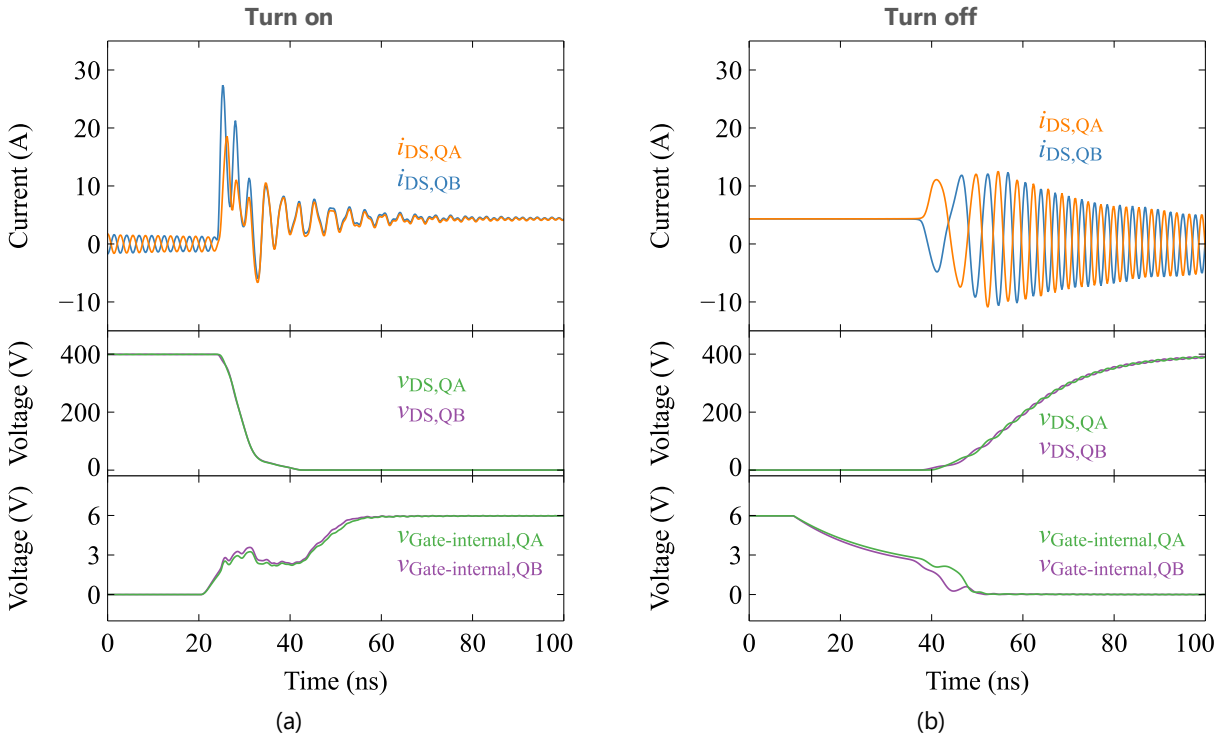


Figure 24 – Simulation results showing the effect of Q_G mismatch considering circuit parasitics. Device details: $C_{GS,QA}$ > $C_{GS,QB}$ with 20% mismatch. Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω.

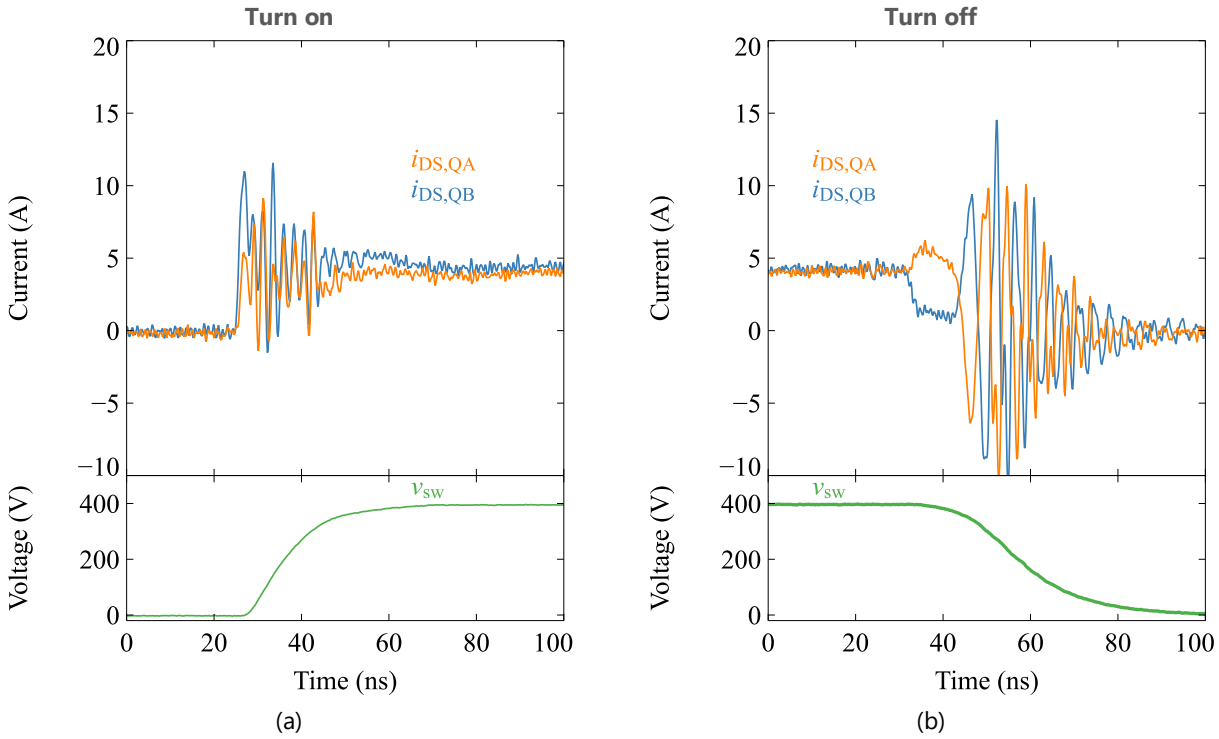


Figure 25 – Experimental results showing the effect of Q_G mismatch. Device details: $Q_{G,QA}$ > $Q_{G,QB}$. Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; $R_{G\text{-}on}$ = 51 Ω.

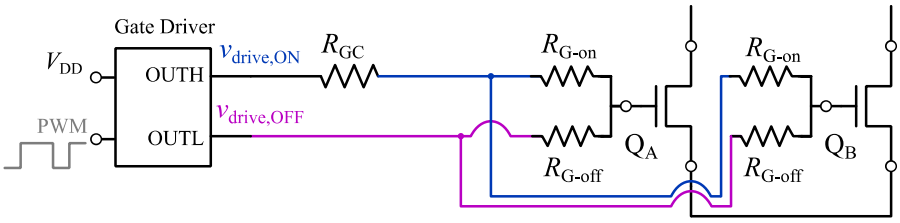


Figure 26 – Inclusion of a common gate resistance (R_{GC}) to counter Q_G mismatch.

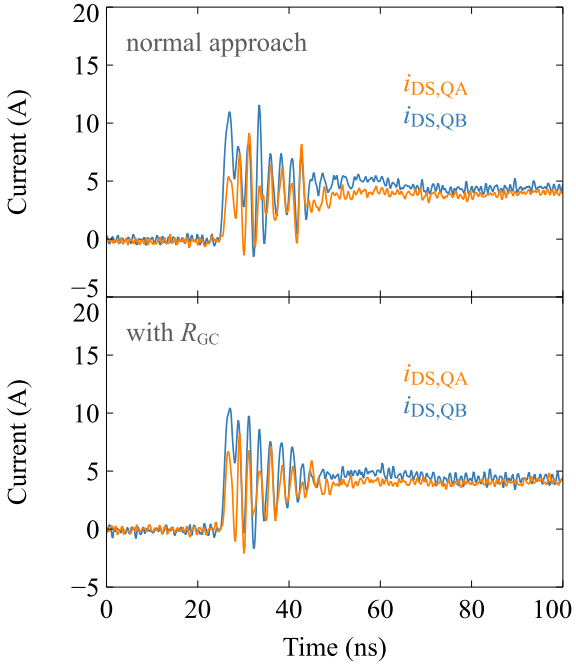


Figure 27 – Experimental results showcasing the improved current sharing by adding a common gate resistance (R_{GC}), followed by separate gate resistances. Conditions: V_{dc} = 400 V; R_{load} = 47 Ω; R_{GC} = 24 Ω; R_{G-on} = 5 Ω.

The common resistance is chosen to be large, where the individual resistors to be much smaller ones. The values of the resistances need to be adjusted to get the original time constant. This solution is employed experimentally, and the results are plotted in **Figure 27**. A clear improvement can be observed for the turn-on current sharing between the two devices.

In addition, by employing R_{GC}, a larger tolerance can be accepted for R_{G-on} tolerance.

3.3 Double-Pulse-Test (DPT) and No-load-Buck Circuit Results

To conclude the discussion on parallel operation in practice, we have considered two experimental test circuits that have employed two ICeGaN devices in parallel configuration. **Figure 28 (a)** plots drain currents, load current and switching-node voltages for a double pulse test (DPT) circuit, highlighting current sharing performance under hard-switching conditions. **Figure 28(b)** shows the same waveforms for a no-load buck circuit to underline the soft-switching operation. Both circuits show good current sharing between the two paralleled devices.

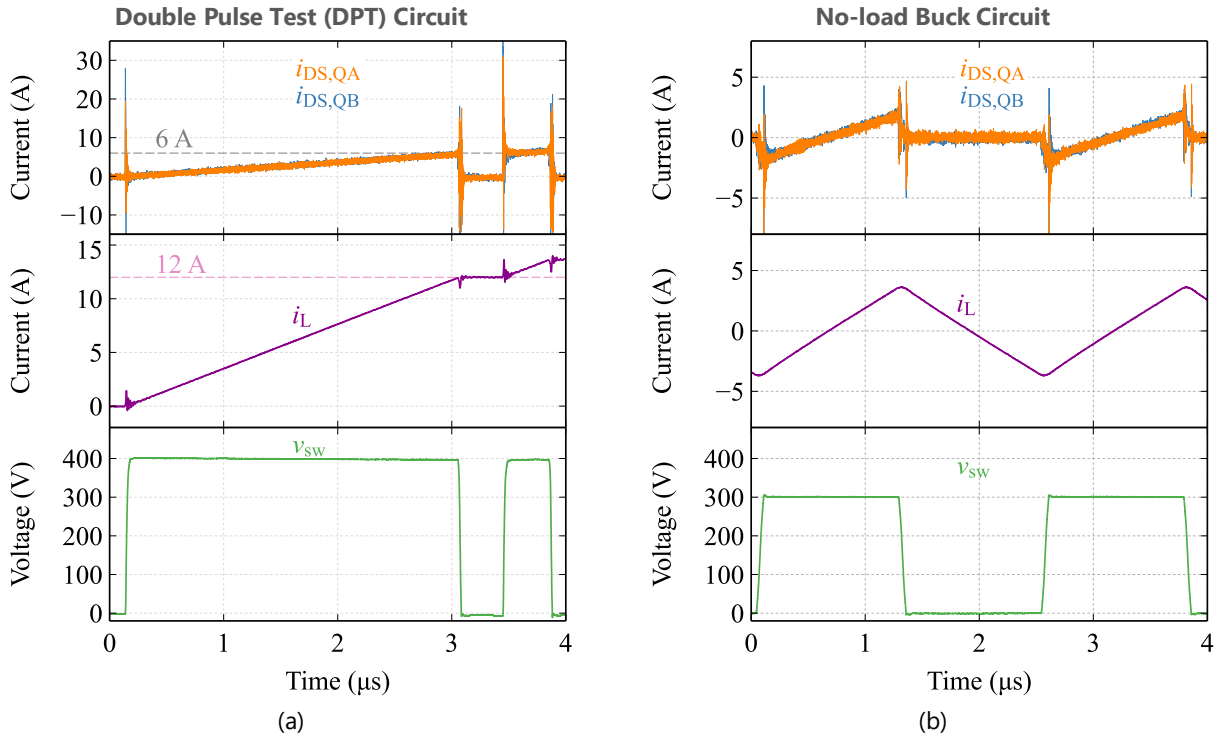


Figure 28 – Experimental waveforms demonstrating the current sharing of top two devices A and B. Figure (a) shows results for a double-pulse-test (DPT) circuit with the conditions V_{dc} = 400 V, i_L = 12 A, L_{load} = 100 µH. Figure (b) shows results for no-load buck circuit, which operates with zero-voltage-switched (ZVS) turn-on; the related conditions are V_{dc} = 400 V, L_{load} = 22 µH, C_{load} = 10 uF, f_{sw} = 400 kHz and T_{dead} = 100 ns. For both circuits R_{GC} = 24 Ω; $R_{G\text{-}on}$ = 5 Ω.

4 Design Recommendations

This section summarises design and layout recommendations.

4.1 Design Guidelines

- Decide the on the number of devices that can be paralleled for a given f_{sw} or vice versa.
    - The number of devices that can be paralleled will be limited if there are constraints on total power loss; because, beyond a certain switching frequency (f_{sw}^{*}), total power loss P_Q due to n devices in parallel will be greater than P_Q due to n-1 devices. See **Section 2.2** for more details.
- For each set of devices connected in parallel, make sure the gate-driver sub circuit can support required P_{drive} and I_{source}. Use **Figure 7** in **Section 2.3** as a guideline.
- A common gate resistance (R_{GC}) approach is recommended to counter any mismatches in Q_G among the devices connected in parallel.
- The lower the value of the effective turn-on gate resistance, the better the sharing of turn-on energy loss between the paralleled devices. However, care should be taken not to reduce turn-on gate resistance to significantly low values (2 Ω or below) as it could introduce substantial oscillations to the gate loop.

4.2 Layout Guidelines

- Design the PCB layout maximising the thermal cross coupling between the devices connected in parallel, i.e., minimize the thermal impedance between the device in parallel.
- Aim for a highly symmetric layout with regard to
    - the positive rail to switch node and switch-node to power ground.
    - The paralleled devices and corresponding gate drive subcircuit.
- At minimum, use a 4-layer design and aim to have the power-loop return path on the first inner layer.
- Minimize the overlap area between the switch node and the power ground.

5 Conclusion

This application note has discussed parallel operation of GaN HEMTs (with special focus on ICeGaN™ devices) with details of current sharing in static and dynamic conditions. In static/conduction conditions, the initial current sharing is influenced by the $R_{DS(on)}$ variation of devices, whilst sharing over time is also affected by thermal cross coupling between the paralleled devices. As thermal coefficient between two devices increases, it increases ΔT and reduces Δi_{DS} between devices.

In dynamic/switching conditions, the initial sharing between devices is impacted by both $V_{GS(th)}$ and Q_G, whilst sharing over time is influenced more significantly by $V_{GS(th)}$ as Q_G is static with temperature. $V_{GS(th)}$ and Q_G variation between devices will result in unequal sharing as the OFF-state device's parasitics are discharged over the turn-on transition. As long as the individual device safe operating area (SOA) is not compromised, sharing during the dynamic/switching period has negligible impact to overall device sharing. As v_{GS} rise and fall times decrease, sharing of current and energy losses improve.

If there are constraints on total power loss, the number of devices that can be paralleled will be limited. Beyond a certain f_{sw}^{*}, the total power loss due to n devices in parallel will be greater than that due to n-1 devices in general.

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