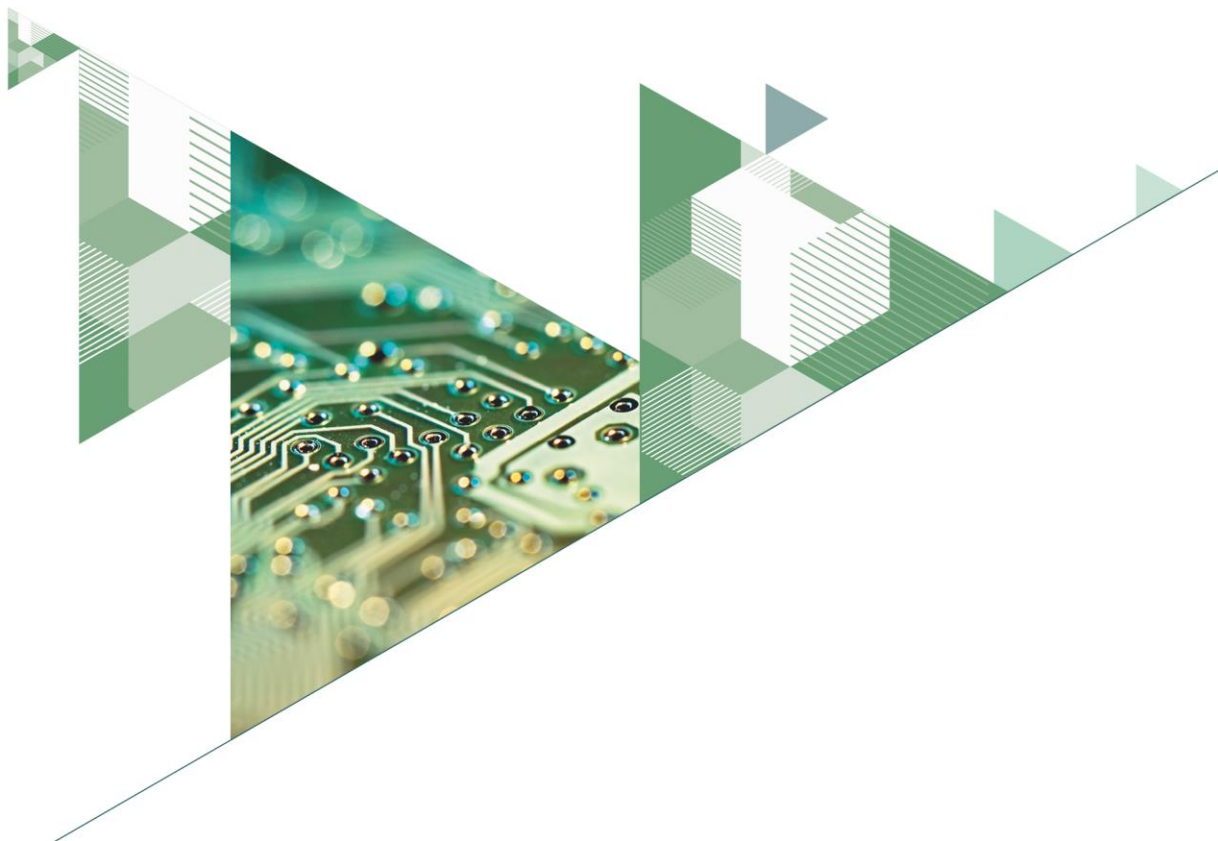




CGD65A055SH2 DATASHEET

H2 series 650 V / 55 mΩ GaN
HEMT with ICeGaN[®] Gate, Current
Sense and NL³ Circuit

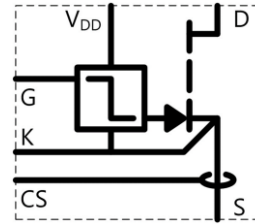
NOVEMBER 2024



H2 series 650 V / 55 mΩ GaN HEMT with ICeGaN® Gate, Current Sense and NL³ Circuit

Key features

- 650 V – 27 A eMode GaN power switch
- ICeGaN® gate technology for high gate threshold, broad gate voltage window and excellent gate robustness
- Gate drive voltage 9 V to 20 V
- Innovative NL³ circuit to boost No Load, Light Load efficiency
- Current sense function
- Integrated Miller Clamp for 0 V TurnOFF
- $R_{DS(on)} = 55 \text{ m}\Omega$
- Suitable for very high switching frequency
- Small 8 × 8 mm PCB footprint
- Bottom side cooled DFN package



Description

The CGD65A055SH2 is an enhancement mode GaN-on-silicon power transistor, exploiting the unique material properties of GaN to deliver high current, high breakdown voltage and high switching frequency for a wide range of electronics applications. The CGD65A055SH2 features CGD's ICeGaN® gate technology enabling compatibility with virtually all gate drivers and controller chips available. The integrated current sense function eliminates the need for a separate current sense resistor in series with the source and the associated efficiency losses. Because no separate current sense resistor connected to source is needed, the device can be directly soldered to the large copper area of the ground plane, improving the thermal performance and simplifying the thermal design. The H2 series ICeGaN® features an advanced NL³ Circuit that leads to near-zero device losses at no-load conditions. It comes in a DFN 8 × 8 SMD package to support high frequency operation while ensuring the highest thermal performance.

Application & Topologies

- Server power
- Telecom rectifiers
- Gaming PSUs
- PC and TV power
- Class D audio amplifiers
- PV inverters
- Motor drives
- LED lighting
- Industrial SMPS
- Energy storage
- Totem pole, CrM boost PFC
- LLC, PSFB, DAB
- Multi-level topologies

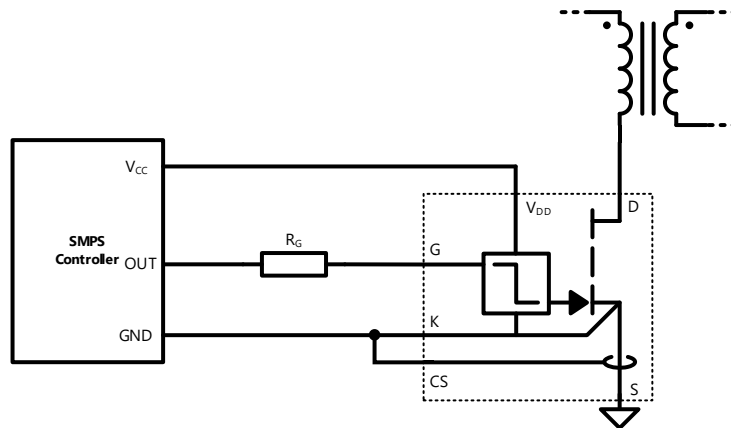
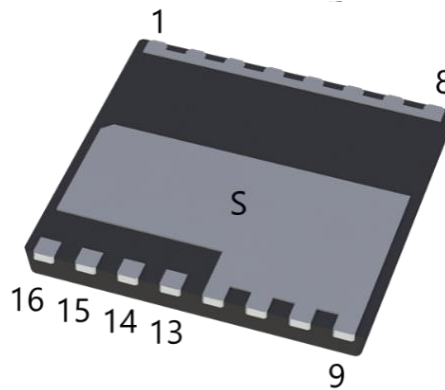


Figure 1. Example of an Application Circuit.



PIN	NAME	DESCRIPTION
1-8	Drain	Power HEMT Drain.
9-12	Source	Power HEMT Source, thermal pad.
13	Kelvin Source	Kelvin Source connection (internally tied to power HEMT Source), reference potential for gate voltage.
14	Gate	Gate signal input. Recommended gate-drive voltage: V_{drive} (V_{GS} in on-state) = 9 V to V_{DD} .
15	Current Sense	Current Sense output, relative to Source, non-isolated. Pin must not be left floating. When not used short it to Source.
16	VDD	ICeGaN [®] gate supply voltage (recommended at 12 V), relative to Source.

Absolute Maximum Ratings

$T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ if not listed.

PARAMETER		VALUE	UNIT
Operating junction temperature	T_J	-55 to +150	$^{\circ}\text{C}$
Storage temperature range	T_S	-55 to +150	$^{\circ}\text{C}$
Drain-to-Source voltage	V_{DS}	650	V
Drain-to-Source voltage - transient ¹	$V_{DS(\text{transient})}$	750	V
Gate-to-Source voltage	V_{GS}	-1 to +20 and $V_{GS} \leq V_{DD}$	V
Gate-to-Source voltage - transient ²	$V_{GS(\text{transient})}$	-1.5 to +21.5 and $V_{GS} \leq V_{DD} + 1.5$	V
Current Sense voltage	V_{CS}	-1.5 to 1.5	V
ICeGaN [®] gate supply voltage	V_{DD}	0 to +20	V
Continuous drain current	$I_{D(\text{continuous})}$	27	A
Continuous drain current ($T_{\text{case}} = 100\text{ }^{\circ}\text{C}$)	$I_{D(\text{continuous})}$	17	A
Pulsed Drain Current (10 μs)	I_{D_Pulse}	60	A
Pulsed Drain Current (10 μs , $T_J = 150\text{ }^{\circ}\text{C}$)	I_{D_Pulse}	35	A

The recommended range of operation for V_{drive} (V_{GS} in on-state) and V_{DD} is 9 V to 20 V, enabling simple integration with a large variety of control chips and gate drivers.

Recommended maximum operating case temperature: $T_{\text{case}} = 125\text{ }^{\circ}\text{C}$.

¹ Non-repetitive pulsed conditions, < 1 ms.

² Non-repetitive pulsed conditions, < 1 ms.

Electrical Characteristics

Values at $T_J = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 12\text{ V}$ if not listed. To turn the device on the recommended gate voltage range is $V_{GS} = 9\text{ V}$ to V_{DD} . To turn the device off set $V_{GS} = 0\text{ V}$. An integrated Miller Clamp eliminates the need for negative gate voltages.

STATIC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Drain-to-Source blocking voltage	BV_{DS}	$V_{GS} = 0\text{ V}$, $I_{DSS} = 20\text{ }\mu\text{A}$	650			V
Drain-to-Source on resistance	$R_{DS(on)}$	$V_{GS} = 12\text{ V}$, $I_D = 2.2\text{ A}$		55	77	$\text{m}\Omega$
Drain-to-Source on resistance	$R_{DS(on)}$	$T_J = 150\text{ }^{\circ}\text{C}$ $V_{GS} = 12\text{ V}$, $I_D = 2.2\text{ A}$		145		$\text{m}\Omega$
Source-to-Drain voltage	$V_{SD(on)}$	$V_{GS} = 0\text{ V}$, $I_D = 2.2\text{ A}$		2.0	3.7	V
Gate-to-Source threshold	$V_{GS(th)}$	$V_{DS} = 0.1\text{ V}$, $I_D = 10\text{ mA}$	2.2	2.9	4.2	V
Gate-to-Source threshold	$V_{GS(th)}$	$T_J = 150\text{ }^{\circ}\text{C}$ $V_{DS} = 0.1\text{ V}$, $I_D = 10\text{ mA}$		2.6		V
Gate-to-Source current	I_{GS}	$V_{GS} = 12\text{ V}$, $V_{DS} = 0\text{ V}$		2.8	3.8	mA
Gate-to-Source current	I_{GS}	$T_J = 150\text{ }^{\circ}\text{C}$ $V_{GS} = 12\text{ V}$, $V_{DS} = 0\text{ V}$		2.2		mA
V_{DD} current (V_{GS} in on-state)	I_{VDD}	$V_{GS} = 12\text{ V}$, $V_{DS} = 0\text{ V}$		1	1.6	mA
V_{DD} current (V_{GS} in on-state)	I_{VDD}	$T_J = 150\text{ }^{\circ}\text{C}$ $V_{GS} = 12\text{ V}$, $V_{DS} = 0\text{ V}$		0.5		mA
V_{DD} current (V_{GS} in off-state)	I_{VDD}	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V}$		70	150	μA
V_{DD} current (V_{GS} in off-state)	I_{VDD}	$T_J = 150\text{ }^{\circ}\text{C}$ $V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V}$		35		μA
V_{DD} start-up current (V_{GS} in off-state)	I_{VDD_start}	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V}$		250		μA
Drain-to-Source leakage current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$		0.7	20	μA
Drain-to-Source leakage current	I_{DSS}	$T_J = 150\text{ }^{\circ}\text{C}$ $V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$		30		μA

The H2 series ICeGaN[®] features an advanced NL³ (No Load, Light Load) Circuit that leads to near-zero device losses at no-load conditions through very low V_{DD} current while V_{GS} is in off-state.

DYNAMIC CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Output capacitance ³	C_{OSS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$		47		pF
Time-related effective output capacitance ⁴	$C_{O(TR)}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		120		pF
Energy-related effective output capacitance ⁵	$C_{O(ER)}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		76		pF
Output charge	Q_{OSS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		48		nC
Output capacitance stored energy	E_{OSS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		6.1		μJ
Total gate charge ⁶	Q_G	$V_{DS} = 400\text{ V}, V_{GS} = 0...12\text{ V}$ $I_D = 10\text{ A}, I_G = 20\text{ mA}$		4		nC
Reverse recovery charge	Q_{RR}			0		nC
Turn-on delay time	$t_{d(on)}$	See Figure 18 and Figure 19		7		ns
Turn-off delay time	$t_{d(off)}$			19		ns
V_{DS} rise time	t_r			5		ns
V_{DS} fall time	t_f			7		ns

CURRENT SENSING

Please refer to the application note CG-AN2206: Current Sensing with ICeGaN®. Please contact CGD for advice on the use of the current sense function.

ESD RATING

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ESD withstand rating	HBM	Human Body Model (per JEDEC JS-001-2017)	2000			V

³ Evaluated using small-signal measurements.

⁴ $C_{O(TR)}$ is the value of fixed capacitance that takes the same amount of charging time as C_{OSS} when V_{DS} changes from 0 V to a given V_{DS} , assuming a constant-current charging process.

⁵ $C_{O(ER)}$ is the value of fixed capacitance that stores the same amount of energy as C_{OSS} when V_{DS} changes from 0 V to a given V_{DS} .

⁶ Turn-on gate charge value is listed. Turn-off gate charge value is lower, because ICeGaN® gate discharges the gate internally.

Thermal Characteristics

Typical values unless otherwise specified.

PARAMETER		CONDITIONS	VALUE	UNIT
Thermal resistance, junction to case	$R_{th(jc)}$		0.8	°C/W
Maximum reflow soldering temperature	T_{reflow}	MSL 3	260	°C

Figures

Figures at $T_J = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 12\text{ V}$ if not specified.

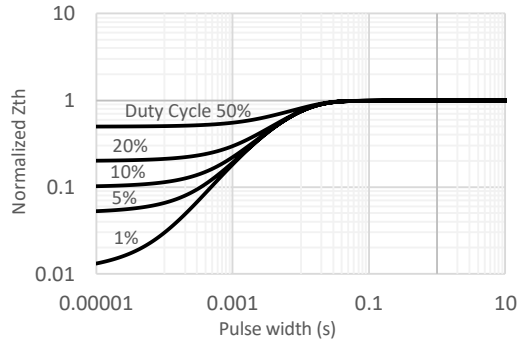


Figure 2. Normalized thermal transient impedance (Z_{thJC}) as a function of pulse width.

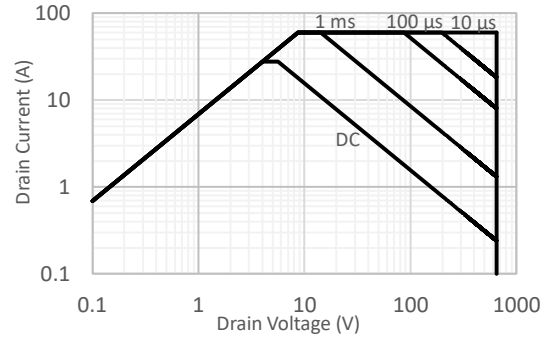


Figure 3. Safe Operating Area (SOA) based on thermal impedance Z_{thJC} at $T_{CASE} = 25\text{ }^{\circ}\text{C}$.

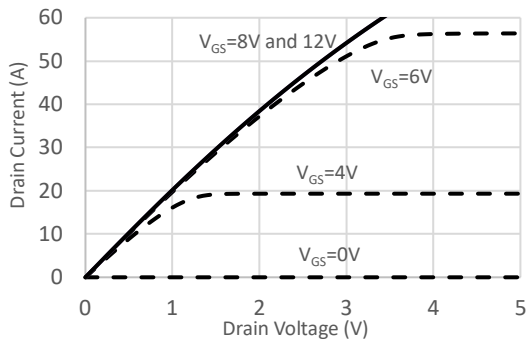


Figure 4. Forward output characteristics at $T_J = 25\text{ }^{\circ}\text{C}$.

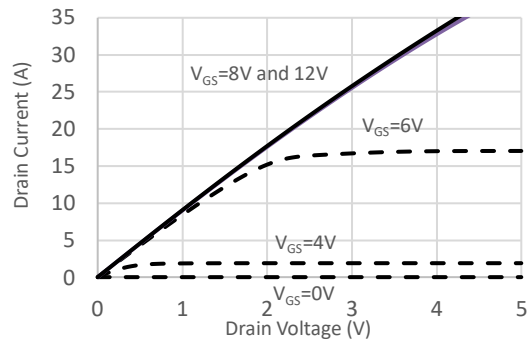


Figure 5. Forward output characteristic at $T_J = 150\text{ }^{\circ}\text{C}$.

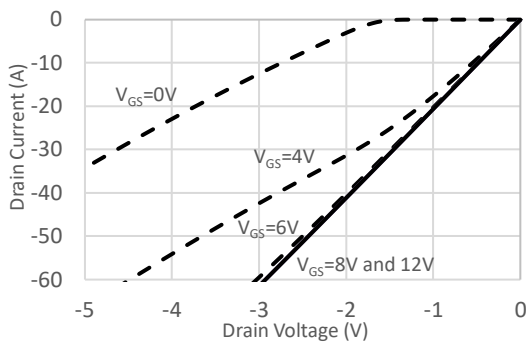


Figure 6. Reverse output characteristics at $T_J = 25\text{ }^{\circ}\text{C}$.

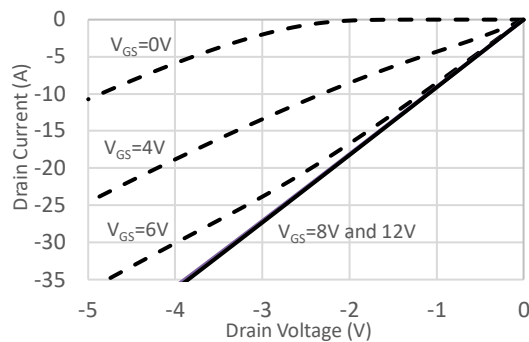


Figure 7. Reverse output characteristics at $T_J = 150\text{ }^{\circ}\text{C}$.

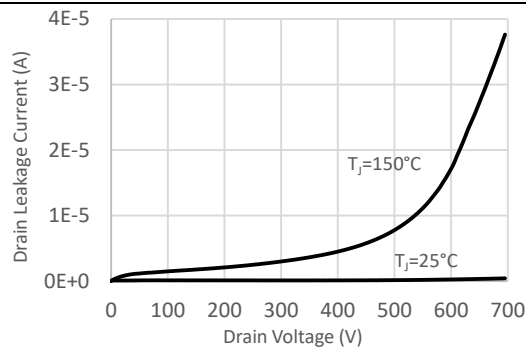


Figure 8. Drain leakage current characteristics at $T_j = 25^\circ\text{C}$ and $T_j = 150^\circ\text{C}$.

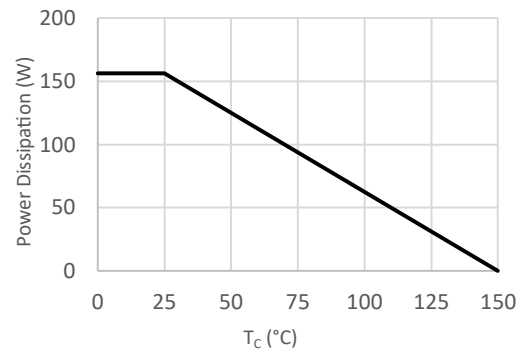


Figure 9. Power dissipation vs case temperature.

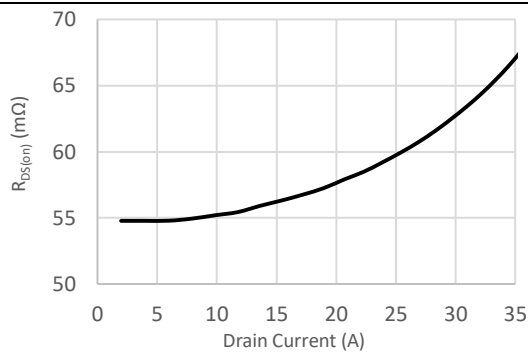


Figure 10. On-state resistance as a function of drain current at $T_j = 25^\circ\text{C}$.

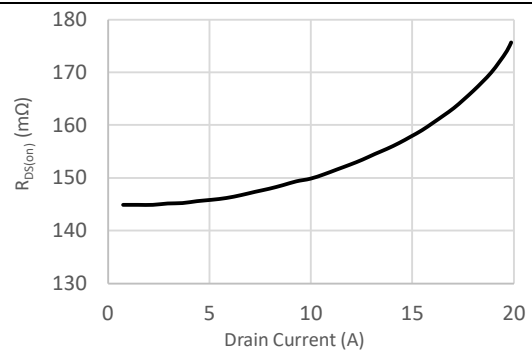


Figure 11. On-state resistance as a function of drain current at $T_j = 150^\circ\text{C}$.

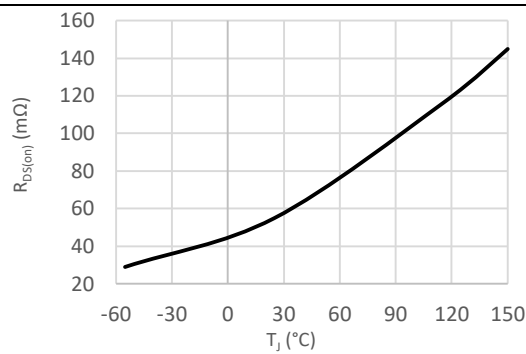


Figure 12. On-state resistance as a function of junction temperature at $V_{GS} = 12\text{ V}$ and $I_D = 2.2\text{ A}$.

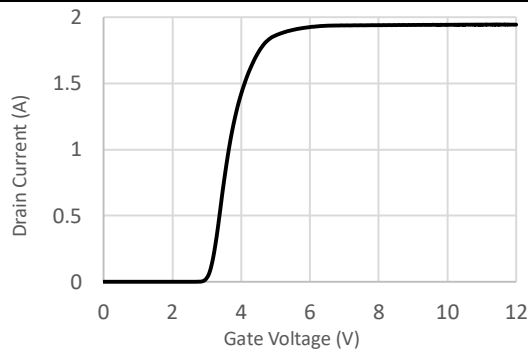


Figure 13. Transfer characteristics at $V_{DS} = 0.1\text{ V}$, $T_J = 25\text{ °C}$.

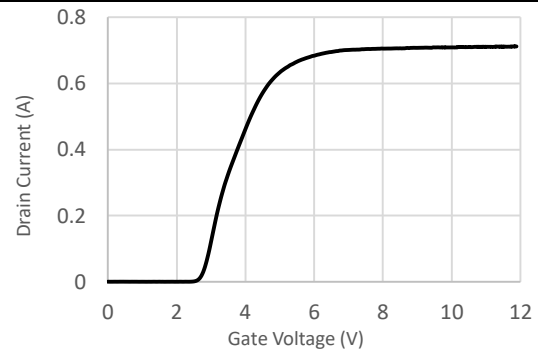


Figure 14. Transfer characteristics at $V_{DS} = 0.1\text{ V}$, $T_J = 150\text{ °C}$.

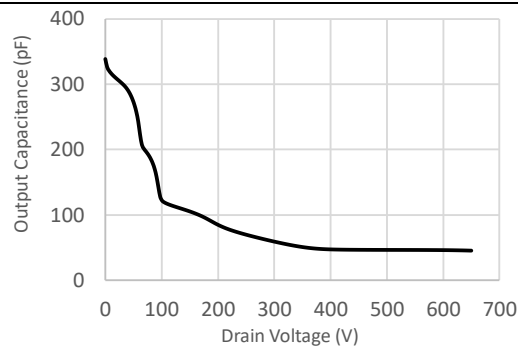


Figure 15. Typical output capacitance C_{OSS} vs. V_{DS} at 100 kHz, $T_J = 25\text{ °C}$.

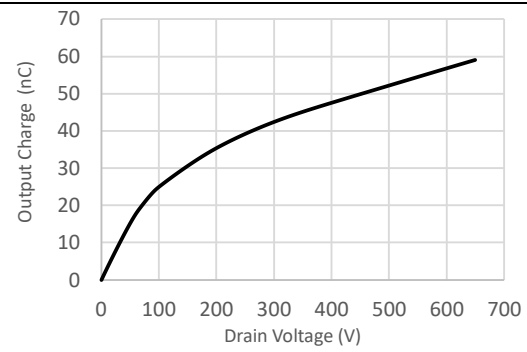


Figure 16. Typical output charge Q_{OSS} vs. V_{DS} at 100 kHz, $T_J = 25\text{ °C}$.

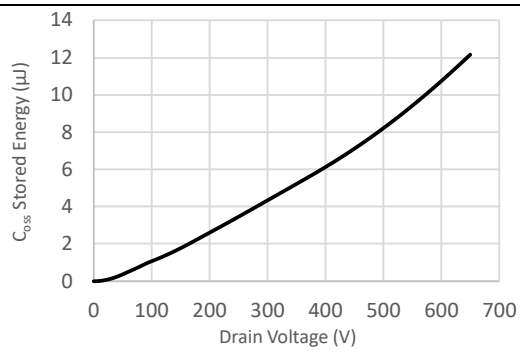


Figure 17. Typical C_{OSS} stored energy E_{OSS} vs. V_{DS} at $T_J = 25\text{ °C}$.

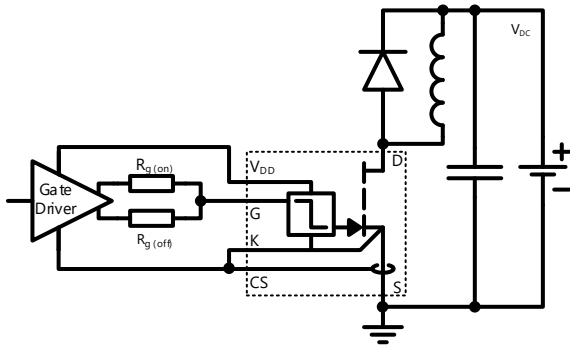


Figure 18. Inductive switching circuit. $I_D = 10\text{ A}$, $R_{g(\text{on})} = 15\ \Omega$, $R_{g(\text{off})} = 2\ \Omega$, $V_{DD} = 12\text{ V}$, $V_{DC} = 400\text{ V}$, $L = 125\ \mu\text{H}$, diode = IDH04G65C5.

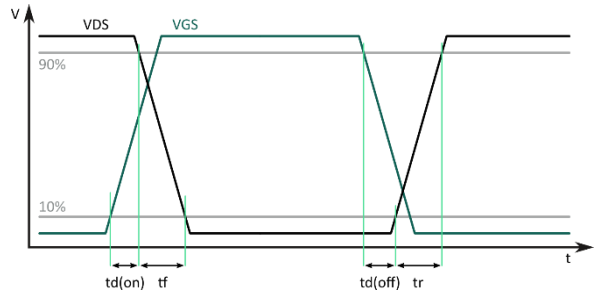


Figure 19. Switching waveform timing definitions.

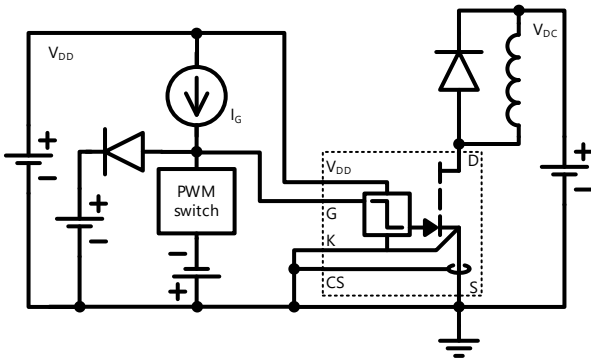


Figure 20. Q_G gate charge characterization circuit. $I_G = 20\text{ mA}$, $V_{DC} = 400\text{ V}$, $V_{DD} = 12\text{ V}$, $L = 125\ \mu\text{H}$, freewheeling diode = IDH04G65C5.

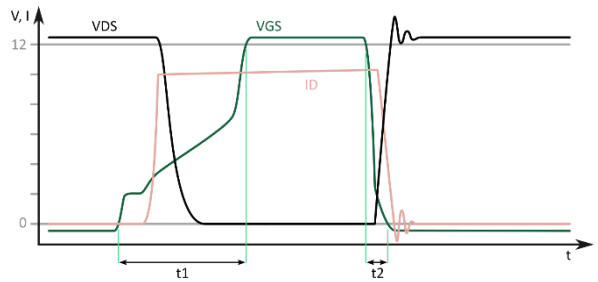
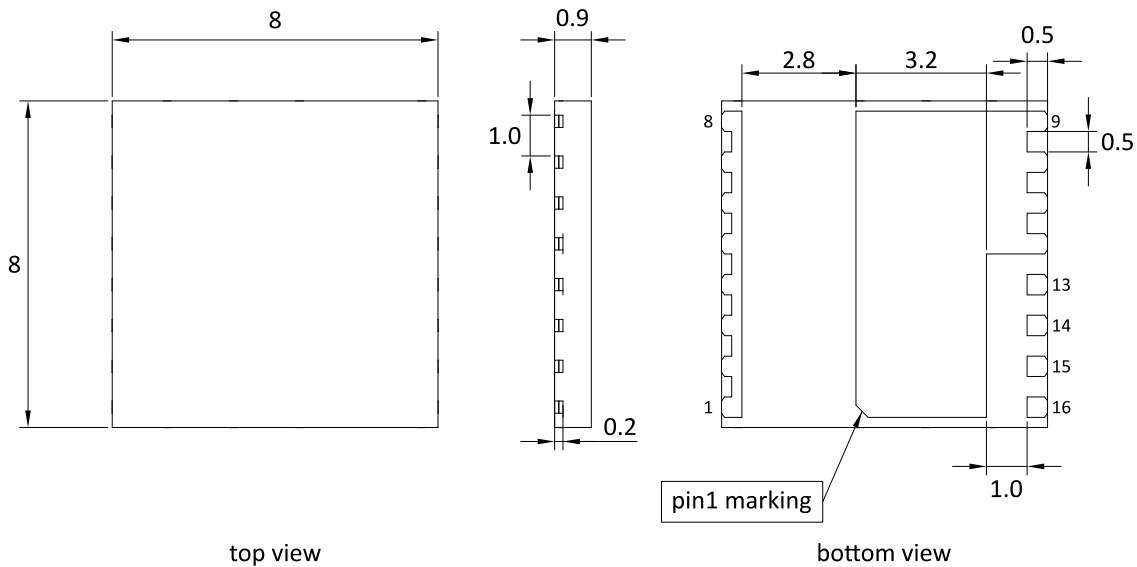
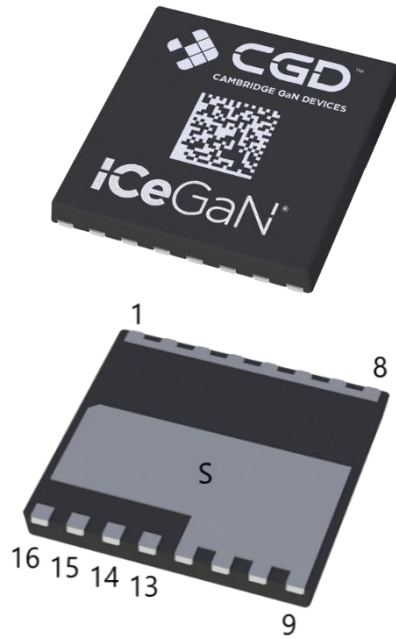


Figure 21. Q_G gate charge characterisation waveform at $I_G = 20\text{ mA}$ and $V_{DD} = 12\text{ V}$. Time intervals t_1 and t_2 indicate the integration boundaries to calculate Q_G from I_G at turn-on and turn-off. Turn-off gate charge is lower than turn-on gate charge.

Packaging

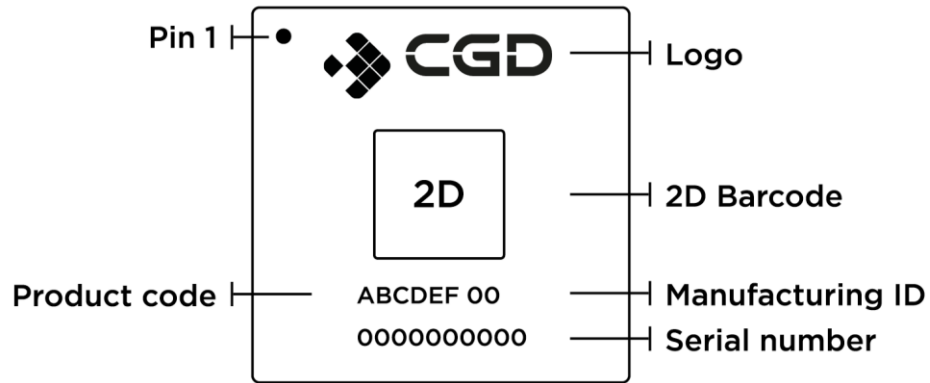
DFN 8 × 8 mm.

PIN NUMBER	NAME
1-8	Drain
9-12	Source
13	Kelvin Source
14	Gate
15	Current Sense
16	VDD



Like any unwanted electronic device, CGD components should be recycled or otherwise disposed of in accordance with local laws and regulations.

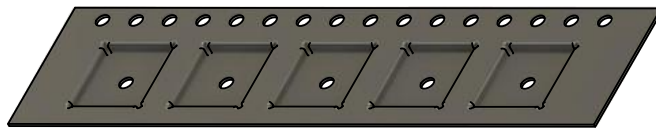
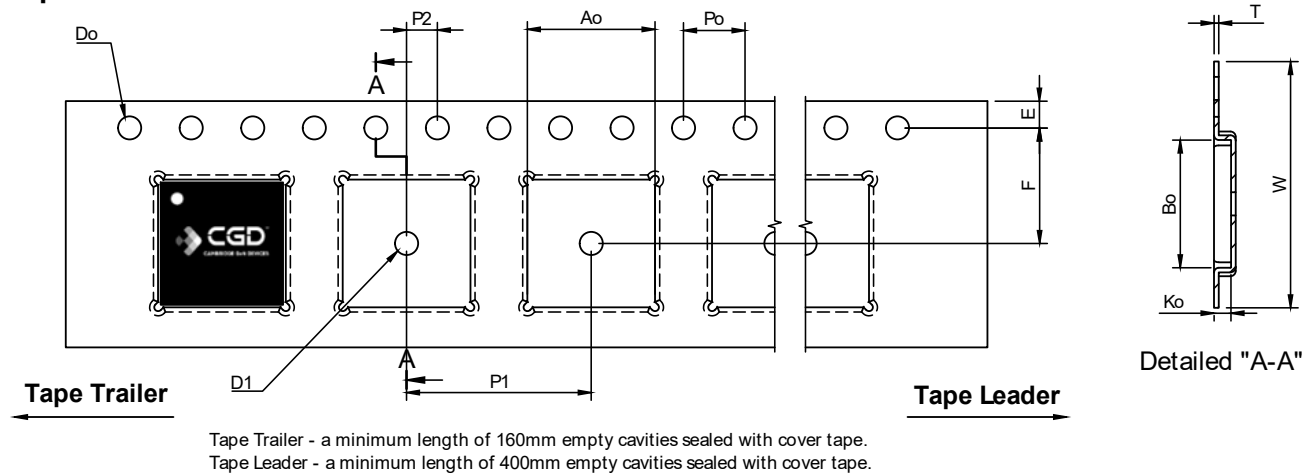
Package Marking:



DFN 8x8

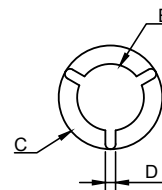
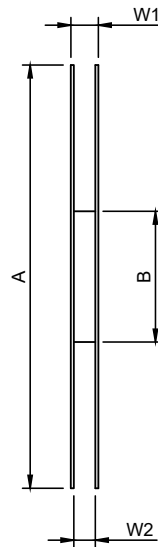
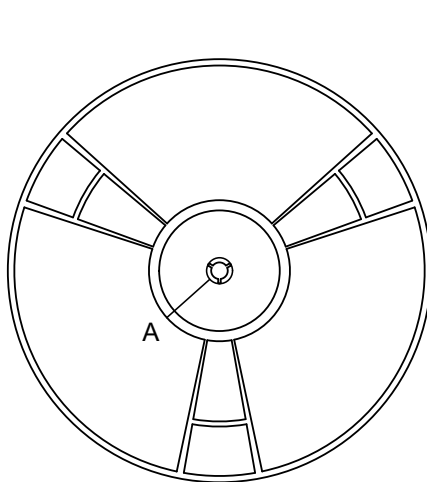
PRODUCT CODE	PART NUMBER
65R1SY	CGD65A055SH2

Tape and Reel Information



Isometric View

Dimensions (mm)		
	Nominal	Tolerance
Ao	8.30	± 0.10
Bo	8.30	± 0.10
Ko	1.25	± 0.05
E	1.75	± 0.10
F	7.50	± 0.10
Po	4.00	± 0.10
P1	12.00	± 0.10
P2	2.00	± 0.10
W	16.00	± 0.3
T	0.30	± 0.05
Do	Ø1.50	+ 0.1 / - 0.0
D1	Ø1.50	+ 0.2 / - 0.0



Detail "A"

13" Reel Dimensions (mm)		
	Min	Max
W1		22.2
W2	16.6	17.1
A	328.0	332.0
B	100.0	104.0
C	20.2	
D	1.5	2.5
E	12.8	13.5

Ordering Information

ORDERING CODE	PACKAGE TYPE	FORM	QUANTITY
CGD65A055SH2-T13	DFN 8 × 8 mm	Tape-and-Reel (13")	3500

Version History

This version is 3.0

VERSION	DESCRIPTION	DATE	BY
1.0	Initial Release	January 2024	JZ, KM
2.0	Added I_D ($T_{case} = 100^\circ\text{C}$) in Absolute Maximum Ratings table, added $C_{O(TR)}$, $C_{O(ER)}$, E_{OSS} specifications and updated the value of $t_{d(off)}$ in Dynamic Characteristics table, added Figure 11, updated the range of Figures 15, 16, 17, added package marking and ordering information, updated tape and reel information.	April 2024	NG
3.0	I_{D_Pulse} value added for 25°C and 150°C to Absolute Maximum ratings table. Updated Figures 3-7 and added Figure 9. Power dissipation.	November 2024	NG, FY

Dare to innovate differently



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