ICeGaN™ IN LLC

APPLICATION NOTE

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IN THIS APPLICATION NOTE

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Abstract

ICeGaN™ can provide application engineers several advantages in the LLC topology. CGD's patented technology allows for the performance advantage of GaN high electron mobility transistors (HEMTs) while maintaining the easy drivability of Silicon MOSFETs. This application note will discuss the basics of designing an LLC and then provide a practical example of this implementation using a 'conventional' analogue controller intended for use with silicon MOSFETs. The use of an analogue controller allows for the development of DC-DC converters in a fraction of the time, and at a fraction of the cost when compared to development with a digital controller, while giving the engineer the confidence in the reliability of the solution, given the analogue IC is widely accepted and adopted in the market. ICeGaN™ is ideally suited to half bridge LLC designs with such a driver, as CGD's patented technology gives the low switching capacitance and zero Q_{rr} of GaN while enabling uncompromised gate compatibility. This allows designers to push up switching frequency and increase density without requiring a complicated and lengthy development cycle using a digital controller.

Introduction

LLC is a widely used DC-DC topology in the mid to high power range for switch mode power supplies (SMPS). It is particularly tailored to environments where input and output voltages can be considered relatively stable. This is often the case in data centres where the LLC would be followed by other DC-DC converters and in battery chargers where the voltage of the cells is always relatively fixed. Since the LLC is mainly applicable in SMPS >65 W it can be expected the LLC is preceded by a PFC meaning the steady state bulk rail is a fixed value regardless of input mains supply.

To design an efficient and high-density converter it is important to possess an understanding of the topology operation and an awareness of the mathematics governing the converter. This application note provides an initial insight into both, however, it is important to be aware that this document is not intended to be sufficient to enable an engineer to develop a complete LLC design. CGD would recommend consulting additional materials given in the references to form a more complete understanding of the resonant topology. This document is intended to give a high-level understanding of the topology and enable an engineer to understand the advantages CGD ICeGaN™ can give a design engineer.

ICeGaN™ Overview

ICeGaN™ stands for "Integrated Circuit Enhancement GaN". It is a platform based on an enhancement GaN HEMT aimed at lowering losses and running cooler than other "cool(MOS)" solutions, due to its ultra-low specific on-state resistance and very low capacitances. Critically for an applications engineer, ICeGaN™ can be driven in a similar manner to a silicon MOSFET meaning that unlike all other enhancement GaN solutions it is compatible with any silicon-based driver. Its zero reverse recovery losses and very low output charge makes it an ideal choice for high frequency, high efficiency applications.

Presently there are two approaches for e-mode GaN in the market (i) discrete approach and (ii) monolithic approach where the gate driver is fully integrated. Both these solutions have their own shortcomings. The low threshold voltage *(~1.2 V for Ohmic p-GaN gate solutions and 1.7 V for Schottky p-GaN gate devices)* specific to p-GaN enhancement mode devices requires negative drive voltages to limit false turn-on events of the HEMT during high dV/dt transients. The full driver integration, on the other hand, while providing reduced parasitics, takes away the flexibility of using low-cost, high-performance silicon-based drivers, or gate drivers integrated with powerful controllers. Additionally, due to on-chip thermal coupling, the gate driver can suffer from extra losses due to the self-heating of the power device. Scaling up a fully integrated solution to higher power levels is also questionable.

In contrast, the ICeGaN™ devices have a higher threshold voltage, V_{th}= 2.5 V in order to suppress dV/dt related spurious turn-on events and as a result allow safer operation. Moreover, the ICeGaN™ devices can be driven with gate voltages of up to 20 V (well in excess of the standard 7 V for enhancement mode p-GaN HEMTs) without any compromise in the device transconductance or dynamic performance.

For more information on the driving of ICeGaN™ please consult our device datasheet.

Half Bridge Resonant LLC

OVERVIEW OF THE BASIC CIRCUITS OF AN LLC.

Figure 1 shows the basic topology of a half bridge resonant LLC. The converter can be split into three key stages. Firstly, the half bridge which generates a square wave voltage from the DC supply. Secondly the resonant tank (L_r, C_r and the transformer) which delivers the power through the transformer's isolation to the output side and enables the zero-volt switching of the primary devices (Q_1 and Q_2), essential to the efficiency performance of the LLC topology. Finally, the output rectifiers and filter which convert the alternating voltage from the transformer back into DC for the output.

LLC converters are only efficient when operated around a narrow window of input and output voltages. This will become apparent in subsequent sections when discussing the voltage gain function, but for now it is essential to consider the consequence of the fact that LLC resonant topologies are in effect a fixed voltage converter. LLC can only be used in a circuit where both the input bulk rail can be considered fairly fixed in voltage and, while output load can change in magnitude dramatically, output voltage is also stable. This makes it ideal for use in applications such as high-power battery chargers where the converter is preceded by a PFC and the load is extremely voltage stable. It would not be well suited to USBPD as this requires multiple output voltages at different loads.

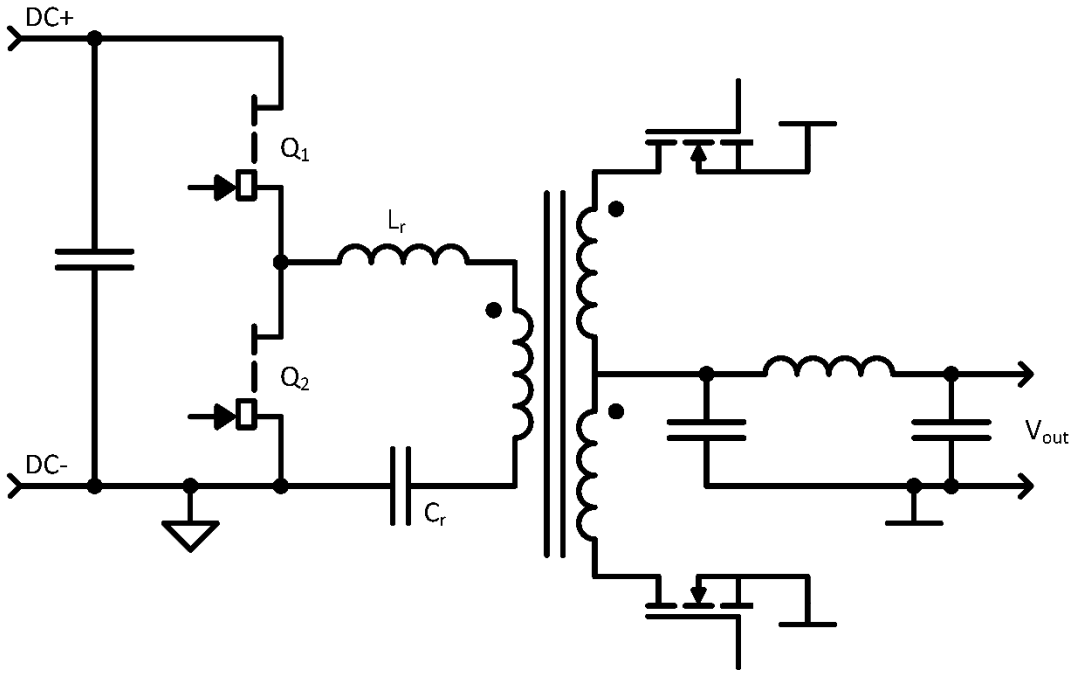

Figure 1 - Basic LLC Schematic

RESONANT TANK DESIGN

The most critical area of design for an LLC is the resonant tank. In the case of an LLC this comprises of three parts - a resonant inductor, a resonant capacitor, and a magnetising inductance. The primary fundamental parameter of the resonant tank is the series resonant voltage depicted in equation 1.

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad (1)$$

At series resonant frequency the tank, and therefore the converter, is load independent. It is always desirable to operate the LLC around the resonant frequency as at this point the current flowing through the transformer is purely sinusoidal and the conventional mathematical modelling of the LLC largely holds true. Away from series resonance, the current becomes increasingly distorted. This will be explained further in following sections.

At f_0 the secondary current commutates as the primary side HEMTs switching begins. This means the primary current is equal to the magnetising current at the moment of switching. There needs to be a small deadtime to enable ZVS of the primary side switches and enable the soft commutation of secondary side diodes. The voltage of the half bridge, not shown in the plot, switches just prior to the reversing of the magnetising current for all cases around f_0. Please note these currents are representative only.

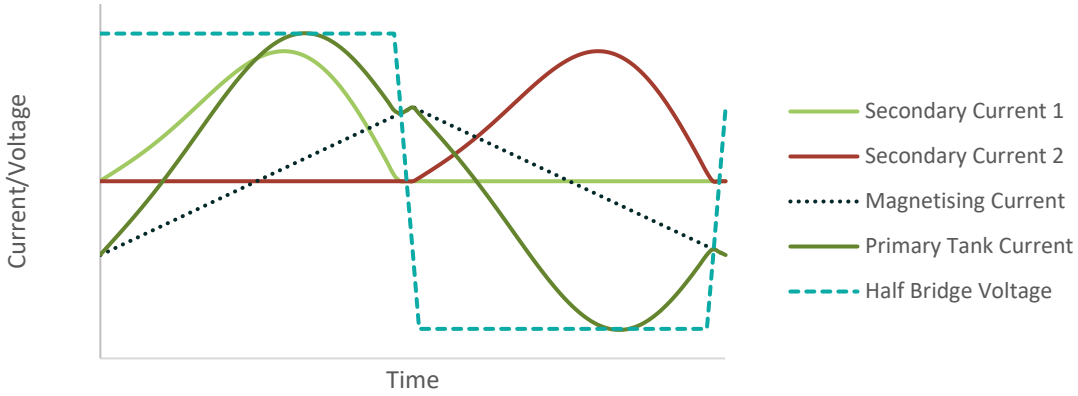

Figure 2 - Representation of Currents at Series Resonant Frequency

Below f_0 the secondary current commutates before the end of the switching cycle. This means there is a period where the primary current is purely equal to the magnetising current and there is no power being delivered to the secondary. ZVS can still be achieved in the primary side devices provided the frequency does not drift too low and enter the capacitive region. Since the secondary devices commutate before the end of the switching cycle, to achieve the same output power the circulating current in the resonant circuit must be larger than at f_0 resulting in larger conduction losses.

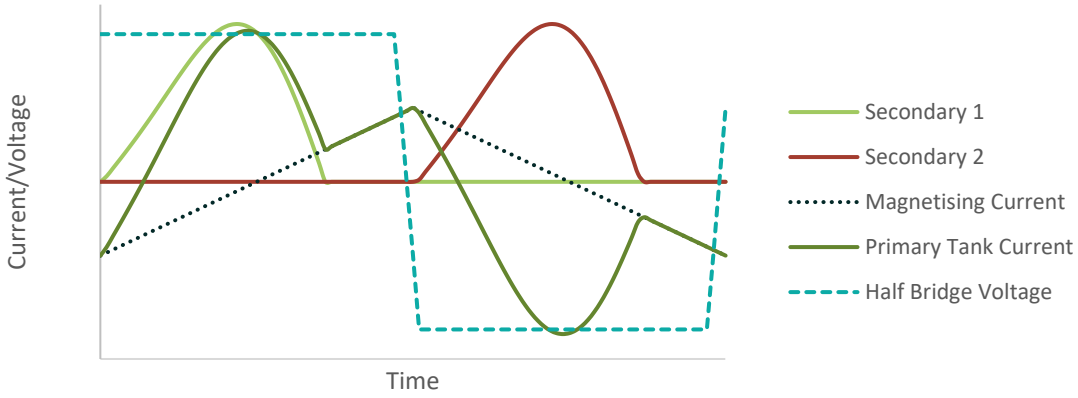

Figure 3 - Representation of Currents Below Series Resonant Frequency

Above f_0 the secondary side is still conducting as the polarity of the primary side switches. In this state the converter is in a continuous conduction mode. While this means the circulating current in the resonant circuit is lower, the output diodes are not softly commutated, and a reverse recovery event will exist.

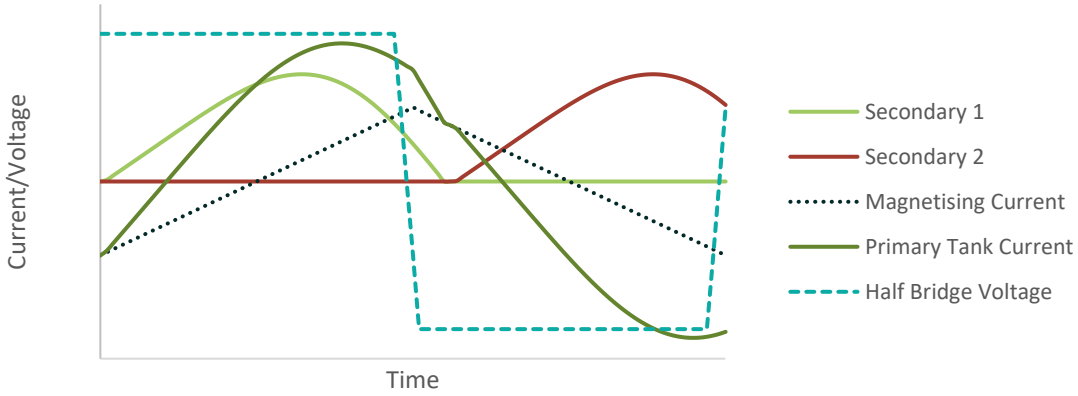

Figure 4 - Representation of Currents Above Series Resonant Frequency

VOLTAGE GAIN FUNCTION

As mentioned previously, it is essential to operate the LLC around the series resonant frequency. At this point, the output voltage is given by equation 2.

$$V_{out} = \frac{M_g V_{in}}{2n} \qquad (2)$$

Where n is the turns ratio of the transformer and M_g is the gain function of the resonant tank. The voltage gain function will be explored further below, but for now lets consider that at f_0, M_g=1.

In order to understand the implications of the voltage gain function first its magnitude must be plotted.

$$M_g = \left| \frac{L_n f_n}{\left[{f_n}^2 (L_n + 1) - 1 \right] + j\left[f_n Q_e L_n ({f_n}^2 - 1) \right]} \right| \qquad (3)$$

where

$$f_n = \frac{f_{sw}}{f_0}, \qquad Q_e = \frac{\sqrt{L_r / C_r}}{R_e}, \qquad L_n = \frac{L_m}{L_r}, \qquad R_e = \frac{8n^2}{\pi^2} R_L \qquad (4)(5)(6)(7)$$

It is important to reiterate exactly what these variables represent before moving on.

M_g represents the normalised change in gain permissible under different load and resonant tank conditions. Due to LLC being only suitable in topologies where V_{in} and V_{out} are both fairly fixed, M_g is usually in the vicinity of unity under normal operating conditions.

R_e is the secondary side load reflected onto the primary. Many topics discussed will talk about changing load but under extreme conditions max load is usually considered.

Q_e can be viewed as the relationship between tank current and load current. As Q_e increases tank current decreases and operational range can increase.

Since M_g is a function of three variables, plotting the relationship of M_g with other changing parameters requires multiple plots. Varying frequency is the method of control for an LLC, and so the x axis will always be f_n.

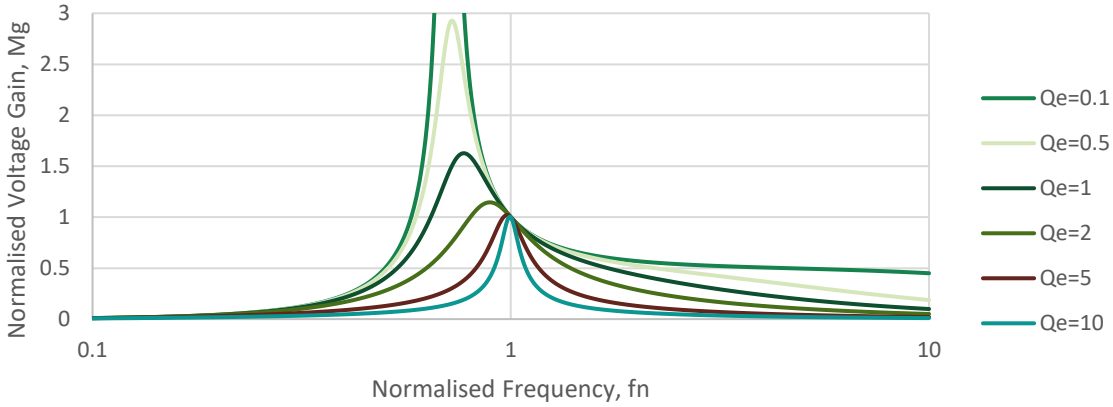

Figure 5 - M_g vs f_n for L_n = 1

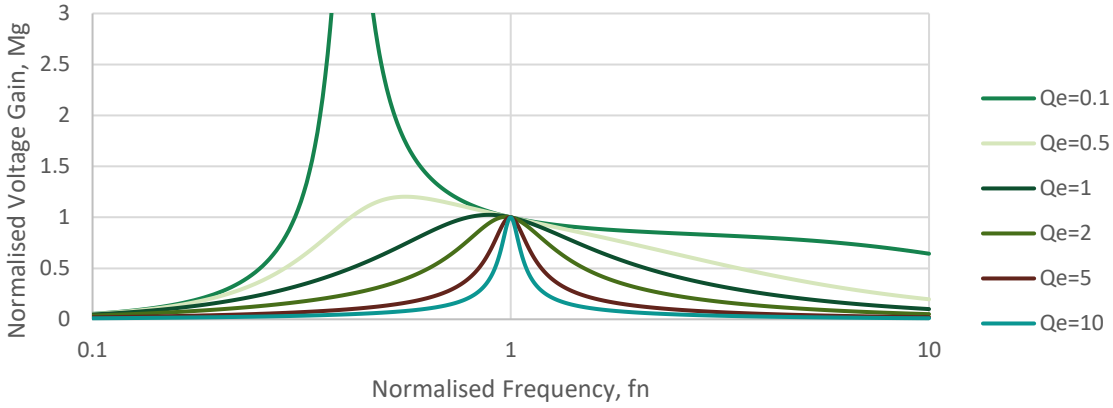

Figure 6 - M_g vs f_n for L_n = 5

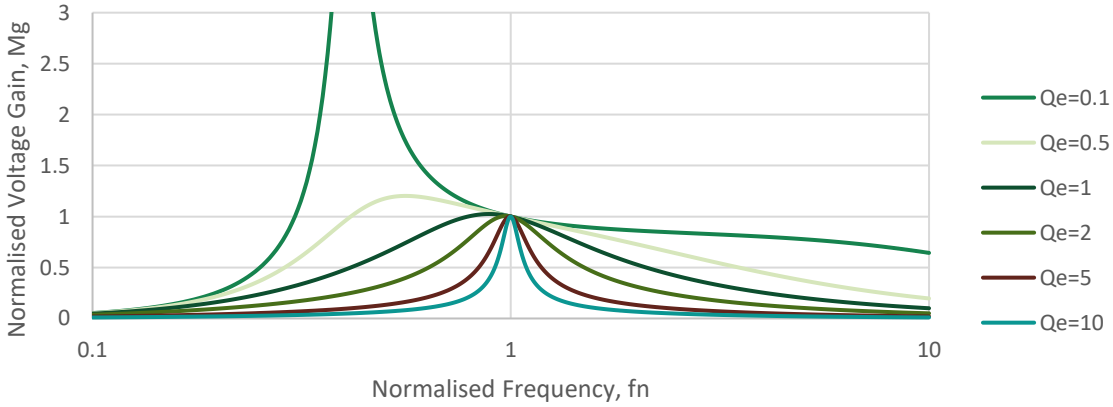

Figure 7 - M_g vs f_n for L_n = 10

There are a few key points that can be extracted from the plots. As Ln increases, for a given load (Q_e), peak gain decreases. However, as Ln increases the controllability of the circuit improves as the

frequency range over which a given change in gain is achieved widens. Further, as load increases peak gain of the circuit decreases.

Thus far is has been assumed that both input and output voltage are fixed. This of course may not always be the case and consequently it is important to set Q_e such that at full load the required peak gain can be achieved under the worst-case voltage conditions. Conventionally, output voltage is controlled and will be assumed to remain fixed across all conditions. The maximum required M_g is therefore defined as;

$$M_{g(\max)} = \frac{V_{in(nom)}}{V_{in(\min)}} M_{g(nom)} \qquad (8)$$

The final key point that can be extracted from the M_g vs f_n plot are the conditions required for ZVS to be achievable. ZVS is only achievable in the inductive region. The inductive region can be found on the curve at any frequency greater than that which gives the peak gain for any load. Operation in the inductive region is essential for efficient operation of the LLC as without it switching losses are incurred within the primary side devices and further, when in the capacitive region primary side currents are larger resulting in increased conduction losses.

The peak gain on a given load line sets the minimum permissible frequency of the converter under that specified load condition. For ZVS to be achieved the magnetising current at the point of switching must be sufficient to allow the drain source voltage of the HEMT turning on to collapse to zero. Deadtime must be sufficient to allow for this to occur. Required deadtime will depend on the magnetising current, and also the capacitance of the primary side switches. This is a parameter where CGD GaN can hold an advantage over its silicon counterparts due to the extremely low output capacitance of GaN HEMTs. Either tank current can be significantly smaller while satisfying equation 9, resulting in less conduction loss, or the inductor values can be reduced implying the possibility of a smaller, more compact design. Most likely, a combination of these two will be balanced to maximise system efficiency and compact design.

To ensure ZVS the following equations must be satisfied.

$$\frac{1}{2}(L_m + L_r){I_{m(peak)}}^2 \geq \frac{1}{2} C_{sw} {V_{in}}^2 \qquad (9)$$

$$t_{dead} \geq 16 C_{sw} f_{sw} L_m \qquad (10)$$

Where C_{sw} is the total capacitance on the switching node (2 x C_{DS} + $C_{parasitic}$).

Further, given the smaller required deadtime, a greater proportion of the switching cycle is dedicated to delivering power to the secondary. This means at any given operating point primary current can be lower, reducing conduction loss and improving efficiency.

SELECTING APPROPRIATE N, L_N, AND Q_E

The first and simplest parameter to fix in any LLC design is the turns ratio of the transformer. This can be calculated simply by rearranging equation 2 and evaluating it under nominal conditions remembering that M_g=1 at nominal. Consequently, equation 2 becomes equation 11 given below.

$$n = \frac{V_{in(nom)}}{2V_{out(nom)}} \qquad (11)$$

The next parameter to address is the resonant frequency. This frequency will dictate the main operating region of the LLC. The equation for this was given in equation 1. It can be seen there are two variables which can be adjusted, L_r and C_r. It would seem from this equation that these can be any combination desirable within the practical limits of being able to wind L_r and source C_r. Unfortunately, it is not quite this simple. In the case of a shorted load on the secondary, the only parameter limiting primary side current is the resonant inductor. This can occur in the case of a shorted secondary, but perhaps more importantly during every start up event. Depending on the switching frequency in this condition the primary side tank current could climb to being extremely large and damage components. Care must therefore be taken to ensure L_r is sufficiently large to prevent this.

Once this is set one can start to address L_n and Q_e. As mentioned previously it is essential to select L_n and Q_e such that sufficient regulation can be achieved. As can be seen from Figure 5, Figure 6, and Figure 7 there are many different combinations of L_n and Q_e that can achieve a given regulation. To better visualise the consequence of adjusting these values the curves have been evaluated at peak M_g in order for them to be plotted on a single curve.

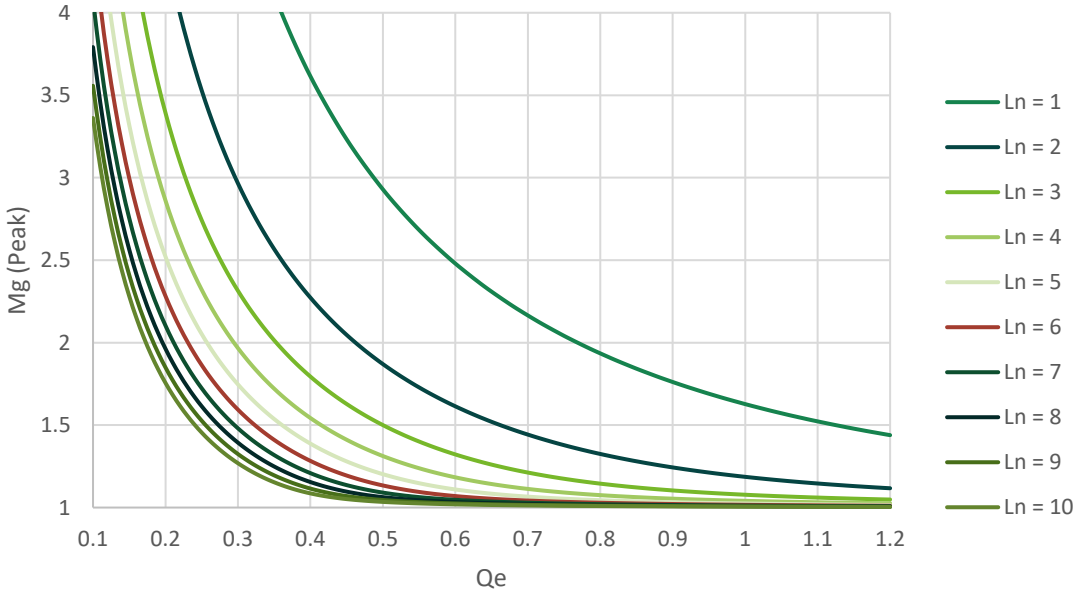

Figure 8 - Peak M_g vs Q_e for Different L_n

Lines of different L_n have been plotted on a graph of Q_e vs $M_{g(peak)}$. Since it is likely several different selections of L_n and Q_e will be available from this graph it is important to understand the consequences of increase or decreasing these parameters.

A smaller L_n for a given Q_e results in a larger peak gain. From equation 6 L_n is the ratio of L_m to L_r. L_r is likely to have been set by the desired resonant frequency and as such the only parameter adjustable here is L_m. As mentioned previously L_m needs to be sufficiently large to allow for ZVS, and also as L_m gets smaller, primary conduction losses increase due to the increased magnetising current. This generates a trade-off between maximum regulation and system efficiency.

A smaller Q_e grants a larger gain for a given L_n but makes load regulation more difficult as smaller increments in frequency are required for a given load change. Further, a given change in load causes

a larger change in control loop gain which in turn can lead to instability and poor transient response. It is probable other circuit parameters have been set which determine Q_e from previous steps. A rule of thumb is that Q_e should be around 0.5, and if it is too far away from this value it is worth changing previously set values.

It is unlikely that an engineer will be able to fix all these parameters on a first pass through and it is expected several iterations will be required to get good calculated results. Even after doing so, it is advisable to use simulation software with the calculated circuit parameters, to ensure performance is as expected.

Design Example

CGD has generated a design example using its 350 W LLC Eval Board. This PCB is designed to allow its customers to be able to rapidly prototype their LLC magnetic designs. The board is set up as default for a fixed 20 V, 17.5 A output although the customer could adjust this as required.

RESONANT TANK DESIGN

To take advantage of CGD's GaN HEMTs, the resonant frequency of the system has been selected to be higher than is conventional on LLC design. In this case we will be choosing ≈250 kHz. As mentioned previously, it is important not to set L_r to be too low such that primary currents can ramp too high during a shorted output condition. L_r is a combination of all the series inductance in the resonant tank. Assuming a discrete component for the resonant inductance, the total L_r will be a combination of the resonant inductor value plus the leakage inductance of the transformer. CGD knows it can expect around 5 µH of stray in its transformer and supposing a total resonant inductance of 25 µH is wanted, a resonant inductor of value 20 µH we will be selected. From the desired f_0, C_r is calculated at 16.2 nF. Shifting this to a component value available on the market, C_r = 18 nF this gives f_0 = 237 kHz.

The next parameter to be set is $M_{g(max)}$. Since output voltage is the controlled parameter in this circuit, V_{out} is fixed at the nominal, $V_{out(max)} = V_{out(nom)}$. Input voltage will, however, change. Given a typical LLC at this power level is preceded by a PFC it is important that the LLC can operate over a range of input voltages. Typically, the minimum voltage is determined by the PFC behaviour under half mains drop out. Here $V_{in(nom)}$ = 380 V and $V_{in(min)}$ = 350 V. This makes $M_{g(max)}$ = 1.09. CGD will set $M_{g(max)}$ = 1.2 to allow for system losses and additional margin.

The turns ratio can be calculated very simply from the two nominal voltages at 9.5. Half a turn is not practical and 9.5:1 represents 19:2 in practice.

Following this, L_n must be set for the given Q_e that can be calculated from the values already selected. With R_e at full load and L_r, C_r and n all defined, Q_e = 0.45. Observing the Q_e vs M_g plot sees that L_n < 5.9.

For plenty of headroom on this parameter L_m will be set to 90 µH.

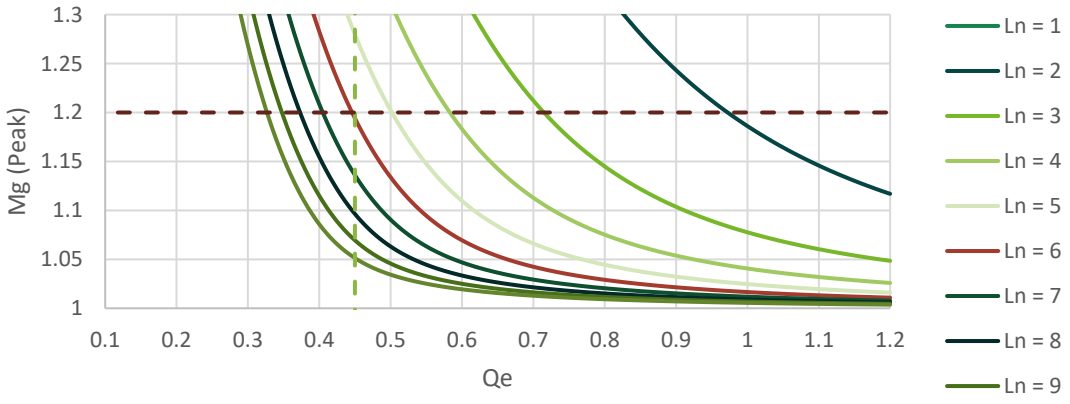

Figure 9 - Required Ln for Output Regulation

CONTROLLER SELECTION

Control of an LLC can be difficult given the requirement of variable frequency for load regulation in this resonant topology. To simplify this as much as possible, CGD has chosen to use the UCC256402 LLC controller from TI. This LLC controller is designed for half bridge LLC and includes built in drivers that switch at ~13 V. The controller requires a number of components to surround it in order to enable its operation and for more information on this CGD advises studying the UCC256402 datasheet, as well as the CGD 350 W LLC User Guide. The important details here are that CGD has selected the nominal voltage to be 20 V output via the feedback loop and has set the LLC operation to begin at 350 V_{DC} on the bulk rail. Note the LLC will continue operating far lower than this once it has begun running.

UCC256402 includes a start-up current source through an internal JFET to charge the controller supply voltage. Once the controller has begun operation this JFET is held off and the low voltage supplies must be derived from an auxiliary winding. This controller also uses the aux winding on the BW pin to observe the SMPS, checking for over voltage condition. An aux winding must therefore be included in any transformer design that uses this controller regardless of intent to use that winding to provide auxiliary power.

In this design example the controller has been set up to enable burst modes for better low load performance.

PRIMARY SIDE DEVICE SELECTION

The primary side devices need to be operational at the primary side DC line voltage. Since this design has a 380 V nominal input, a 650 V device is required. Given GaN HEMTS have a low C_{OSS}, a design using GaN will have a much smaller node capacitance and require a lower magnetising inductance and/or less deadtime in half bridge operation. This enables switching at a much higher frequency than conventional Silicon MOSFETs can support. Further, their lack of Q_{RR} means there are no reverse recovery losses. All of this makes GaN an ideal choice for primary side devices in an LLC. CGD ICeGaN™ enables the driving of CGD GaN, directly from UCC256402, without the need for any additional circuitry. Further, CGD ICeGaN has a significantly smaller input capacitance than similarly sized silicon MOSFETs. This means CGD ICeGaN can significantly reduce gate driver losses on the primary side. Since with ZVS operation, efficiency will be dominated by $R_{DS(on)}$, CGD has selected its 55 mΩ devices to be used in this design.

SYNCHRONOUS RECTIFICATION

To achieve optimum efficiency, it is essential to use synchronous rectification on the secondary side. 80 V, 1.9 mΩ Silicon MOSFETs from Infineon were selected as the switching devices and were paired with the SRK2001 controller from ST. The SRK2001 controller iteratively removes the small period at the end of the conduction cycle where the MOSFET body diode turns back on. This reduces both conduction losses and Q_{RR} losses at the end of the cycle. Further gains could be made by switching from Silicon MOSFETs to low voltage GaN transistors.

Design Example in Testing

The CGD evaluation board platform supports rapid prototyping of different LLC designs. It includes four replaceable PCBs allowing for easy evaluation of alternatives. For more on this see the 350W LLC Evaluation Board User Guide. As supplied, the LLC is set up for 20 V 17.5 A output and uses the UCC256402 controller from TI. CGD GaN HEMTs can be driven directly from this controller, designed for use with MOSFETs thanks to its ICeGaN™ technology. The resonant tank has been set up as discussed above with L_r = 20 µH, L_m = 90 µH and C_r = 18 nH. The secondary rectifiers are 2x1.9 mΩ Silicon MOSFETs from Infineon using the ST SRK2001 synchronous rectifier controller.

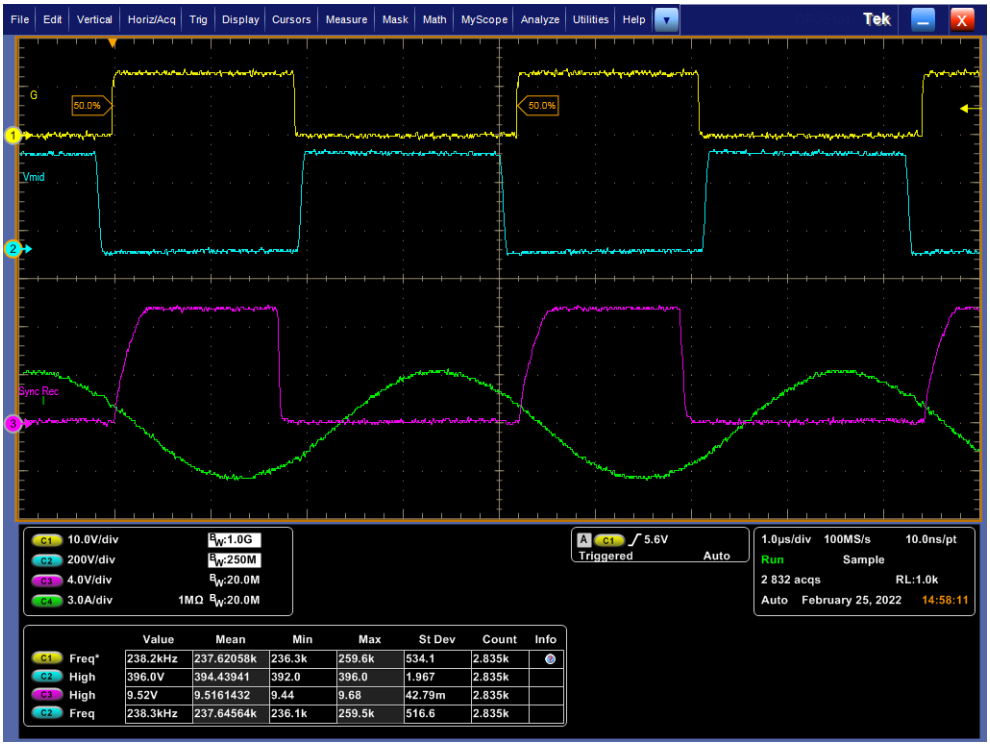

Figure 10 - LLC Eval Operating at 350 W. 2 µs/div.

LS Gate – Yellow (3 V/div), V_{mid} – Blue (100 V/div), Sync Rec Gate – Purple (4 V/div), I_{tank} – Green (3 A/div)

See above the LLC Eval operating at full 350 W output power in Figure 10. V_{in} = 380 V_{DC}, V_{out} = 20 V. Probes are low side gate (yellow), half bridge switching node (blue), synchronous rectifier gate (purple) and primary side current (green). As expected, under nominal input voltage condition the LLC is operating very close to the series resonant frequency and tank gain, M_g, ≈ 1. This can be observed by the near sinusoidal tank current. It can be seen frequency is at 238 kHz under this test condition. The original calculation estimated that f_0 would be at 237 kHz.

See below in Figure 11 a capture of the LLC operational at 100 W. Here secondary current has been captured rather than primary to show the synchronous rectifier operation.

Figure 11 - LLC Eval Operating at 100 W. 1 µs/div.

LS Gate – Yellow (10 V/div), V_{mid} – Blue (200 V/div), Sync Rec Gate – Purple (4 V/div), I_{sec1} – Green (3 A/div)

Features of SRK2001 can be observed. There is a blanking period included by the controller that ignores the initial spike caused by parasitic capacitance on the secondary side. Turning the device on during this condition would worsen system efficiency. Secondly the adaptive turn off can be seen by how close to the end of the conduction period the driver turns off. Adaptive turn off is required to compensate for stray inductance in series with the MOSFETs $R_{DS(on)}$.

Start up into 100 W has been shown in Figure 12. Note the features of UCC256402 where it turns on the low side device for a long period at the start of the first cycle to charge the high side V_{CC} through the bootstrap circuit. Once this fixed period is complete the normal start-up operation of the controller begins. CGD recommends that customers read the UCC25640x datasheet to understand the start up sequence fully.

Please note the irregularly shaped current waveform is most likely an artifact of scope aliasing due to the zoomed out view taken to capture the 'full' start up event.

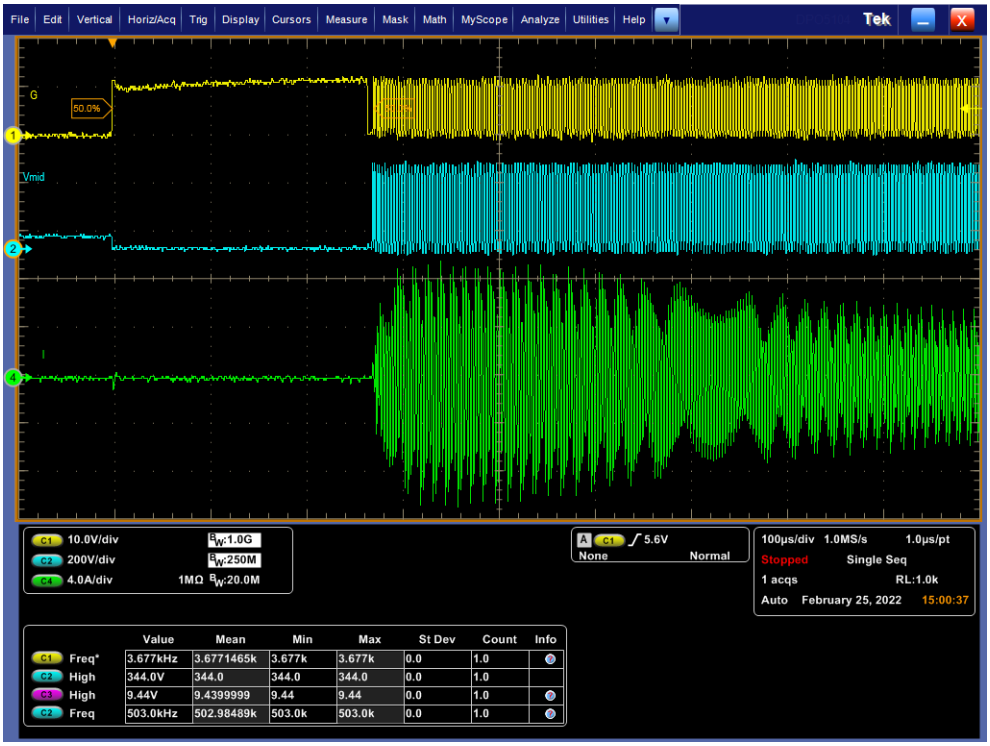

Figure 12 - LLC Start Up into 100 W. 200 µs/div.

LS Gate – Yellow (3 V/div), V_{mid} – Blue (100 V/div), I_{tank} – Green (3 A/div)

To show the stability of the loop and the stability of the output voltage a dynamic load test is shown below in Figure 13. Here load is stepped from 0% to 100% with 4 ms on and 6 ms off.

Figure 13 - LLC 0-100% Dynamic Load Steps

V_{out} – Purple (700 mV/div with 20 V offset), I_{out} – Green (4 A/div)

Conclusion

This application note has presented the main aspects that must be considered when designing a half bridge LLC SMPS stage with ICeGaN™. It has highlighted how CGD ICeGaN™ can provide engineers with an advantage when developing their own designs and given an example of an evaluation board using ICeGaN™.

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Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	JF	09/03/2022

CAMBRIDGE GaN DEVICES

Dare to innovate differently

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