ICeGaN® BHDFN package

Overview

This document describes the bottom sided cooled BHDFN 10 x10 mm SMD package which accommodates the new 25 mΩ and 55 mΩ ICeGaN P2 series.

ICeGaN devices are the CGD easy-to-use 650-V GaN-HEMT devices, which can be directly driven by low-cost Si MOSFET and IGBT drivers.

ICeGaN gate technology offers a high gate threshold, broad gate voltage window, and exceptional gate robustness.
BHDFN package has been optimized for better thermal performance, this package features a thermally enhanced high-power design and a compact 10 x 10 mm^2 PCB footprint. The incorporation of a thick lead frame facilitates superior heat dissipation, critical for a correct operation under heavy loads, making it as thermally efficient as TOLL package.
Further enhancing manufacturability, the BHDFN package includes a wettable flank for automated optical inspection (AOI), streamlining production processes and ensuring stringent quality standards are met.

Contents

Nomenclature

BHDFN	Bottom heat-spreader dual flat no leads
dc	Direct current
I_{DS}	Drain-source current
KS	Kelvin source connection
PCB	Printed circuit board
PFC	Power factor correction
R_{thJC}	Junction to case thermal resistance
R_{thJH}	Junction to heatsink thermal resistance
$R_{thSOLDER}$	Solder thermal resistance
R_{thPCB}	PCB copper vias thermal resistance
R_{thTIM}	Thermal interface thermal resistance
SMD	Surface mount device
T_{amb}	Ambient temperature
T_C	Device case temperature
T_J	Device junction temperature
TPPFC	Totem-pole power factor corrector
TIM	Thermal interface material
UPS	Uninterruptible power supply
V_{DD}	Low-voltage supply to ICeGaN circuitry
V_{GS}	Gate–source voltage
$V_{GS(th)}$	Gate–source threshold voltage

1 Introduction

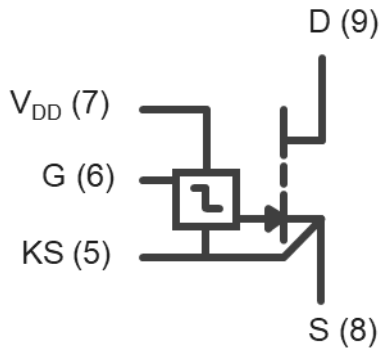
Surface-mount bottom-side cooled BHDFN package benefits from extremely low parasitic inductance and capacitance, which ensures a short path for heat dissipation, thereby minimizing thermal resistance from the junction to the case (R_{thJC}). This results in high thermal performance comparable to TOLL package, making it an appropriate and attractive choice for high-current, high-power–density applications.

In this application note, our focus will be on the BHDFN package housing the CGD65C025SP2 ICeGaN™ (P2 Series 650 V, 25 mΩ). ICeGaN devices are 650-V GaN-HEMT which can be driven like a MOSFET with a standard driver IC. For more information about ICeGaN technology, how to drive it and its advantages, refer to [1] and [2]

2 BHDFN-9-1 features

2.1 Terminal package structure

Figure 1 depicts the internal circuit configuration and the external view of the BHDFN package. ICeGaN in BHDFN package is a 5-terminal / 9-pin device with Gate (G), Drain (D), source terminal separated into Kelvin Source (KS) and Source (S) which is also the thermal pad, and VDD pin. Pins 1 to 4 are not connected (NC), and they can be connected to the source terminal to increase the thermal PCB copper pad size/area on the PCB. The KS terminal can be utilized for the return of the gate signal. The VDD must be supplied with a 9 V to 20 V dc voltage for the correct ICeGaN operation.

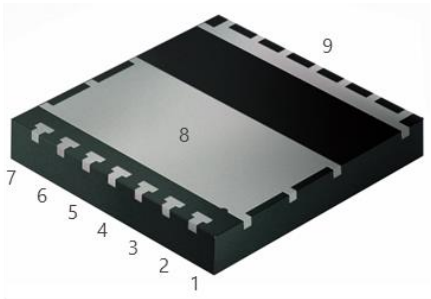


(a)

(b)

Pin number	Name
1, 2, 3, 4	Not connected
5	Kelvin source
6	Gate
7	VDD
8	Source / Thermal Pad
9	Drain

(c)



(d)

Figure 1 – (a) ICeGaN symbol (b) BHDFN top view and pin out (c) ICeGaN pin-out (d) BHDFN bottom view and pin out

2.2 Dimensions

BHDFN is a 10 mm x 10 mm x 1.75 mm surface-mounted package comparable to TOLL, designed for high power applications where efficiency and power density are top priorities. Figure 2 shows the dimensions of this package.

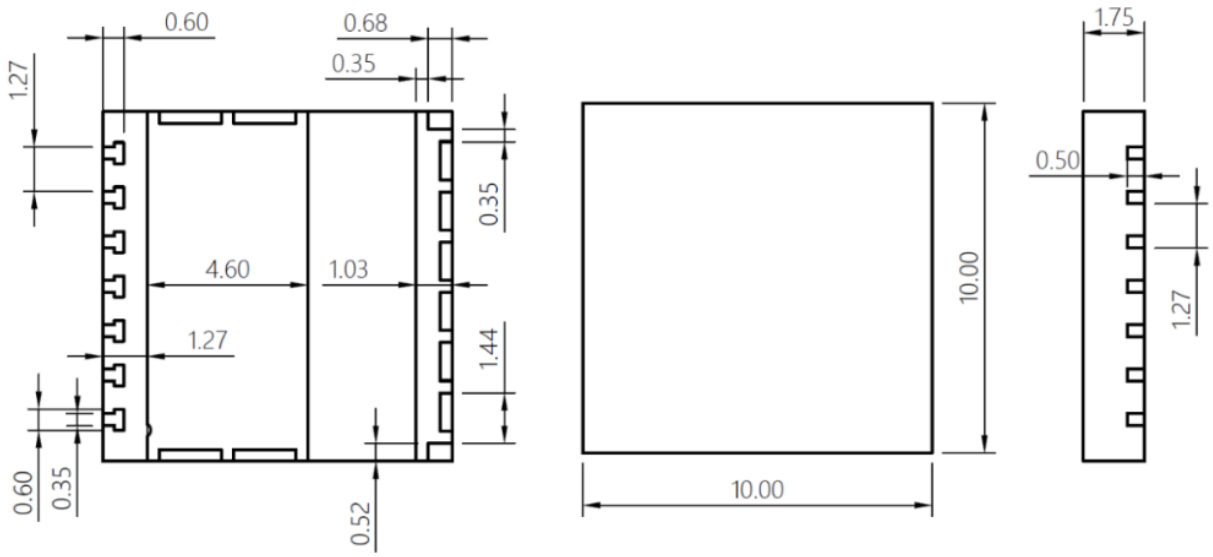


Figure 2 – BHDFN package dimensions in millimetres

BHDFN incorporates a large source-pin thermal pad connection with an area of approximately 45 mm^2.

The BHDFN package features a 3.1 mm creepage between the source and drain pins, which exceeds the 2.795 mm gap found in the through-hole TO-247 package. Higher creepage distance increase safety and reliability of the system design. ICeGaN can be not only considered as a discrete-GaN surface-mounted package replacement but also as alternative to SiC technology in many applications, with BHDFN package emerging as an optimal alternative to the through-hole TO-247 package.

2.3 Thick lead frame for optimum heat spreading

The BHDFN has a thick lead frame, comparable to TOLL package, and thicker than standard PDFN, which facilitates superior heat dissipation. Thermal tests between BHDFN and TOLL packages are described later in section 4 of this document.

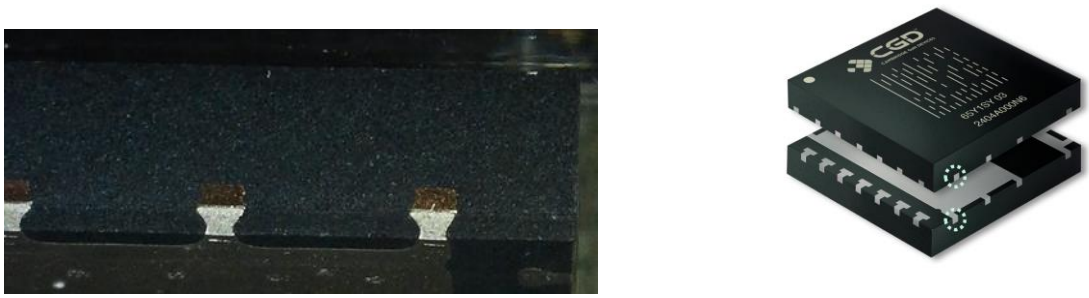
GaN Device	$R_{DS(on)}$ (typical)	Package	R_{thJC}
CGD65C025SP2	25 mΩ	BHDFN	0.28 °C/W
Competitor A	25 mΩ	TOLL	0.53 °C/W
Competitor B	26 mΩ	TOLL	0.27 °C/W

Table 1 – R_{thJC} comparison between BHDFN and TOLL packages from competitors

2.4 Wettable flank for AOI

AOI (Automated Optical Inspection) is utilized extensively in automotive manufacturing and various industrial production lines to scrutinize the integrity of solder joints between chips and printed circuit boards (PCBs). This rigorous inspection process is imperative to ensure that the solder joints meet stringent safety and quality standards. By employing AOI systems, manufacturers can detect defects such as solder bridges, insufficient solder, voids, misalignment, and other anomalies that could compromise the reliability and functionality of electronic assemblies. This proactive approach to quality control helps mitigate risks, enhances product reliability, and ultimately contributes to the overall safety and performance of automotive systems and industrial equipment.

BHDFN package has 22 wettable flanks to simplify visual inspection as well as automated optical inspection (AOI). Pins 1-7 have wettable flanks. The thermal pad, the source pin, has 6 wettable flanks, 3 on each side of the pad. The drain has 7 wettable flanks to ensure the connection is evenly soldered along the drain strip and there are no solder voids. Figure 3 (a) shows a real image of the flanks and Figure 3 (b) highlights one of the flanks on the source pad, illustrating how the flanks are distributed across the package.



(a) (b)

Figure 3 – (a) a real image of wettable flanks (b) wettable flank highlighted on BHDFN package

3 Layout considerations

3.1 Footprint

Figure 4 illustrates the recommended BHDFN footprint.

The PCB copper can also be extended to the NC pins 1- 4 to further increase the number of vias beneath the device to transfer the heat to the heatsink on the other side of the PCB; that allows for the thermal pad of BHDFN to be extended; this is illustrated in Figure 5(a). If needed, it can be easily made as large as the TOLL package thermal pad, see Figure 5(b).

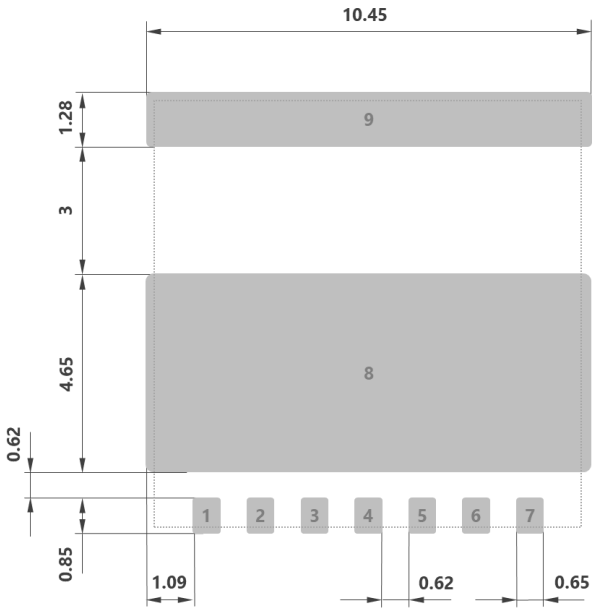
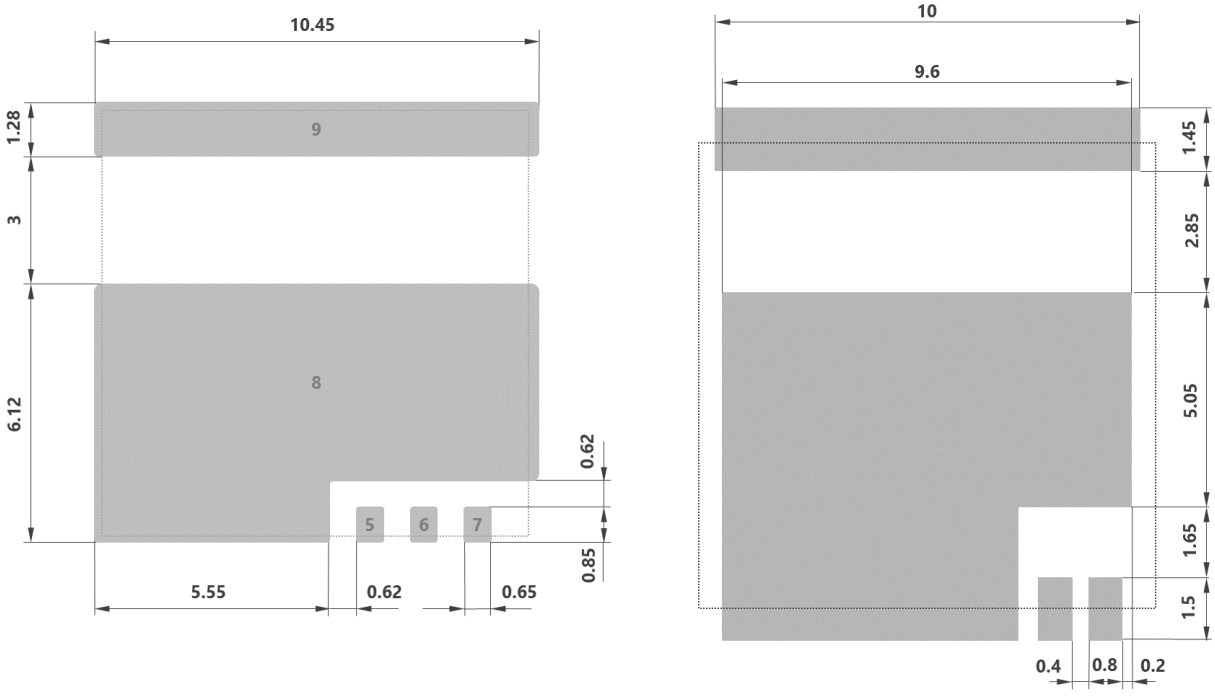


Figure 4 – BHDFN footprint (mm)



(a) (b)

Figure 5 – (a) BHDFN footprint example with extended thermal pad; (b) TOLL footprint for GaN (mm)

3.2 Co-layout with GaN TOLL

BHDFN and TOLL package footprints are very similar as shown in Figure 5. Based on this similarity, a common layout was designed for drop-in replacement and easy evaluation of CGD's products in BHDFN vs other GaN transistors in TOLL packages. We used this co-layout during thermal evaluation of ICeGaN vs TOLL competitors in section 4.1.

Unlike discrete GaN devices, ICeGaN incorporates a VDD pin to power its internal circuitry, allowing for a simple and straightforward external driving solution. In the BHDFN package, the low voltage pins (VDD, G, and KS) are on the same side of the package as a TOLL device. Adapting a common layout for compatibility simply involves a minor adjustment, where the TOLL device is shifted to the left to avoid connecting to the VDD terminal. This is illustrated in Figure 6 and Figure 7.

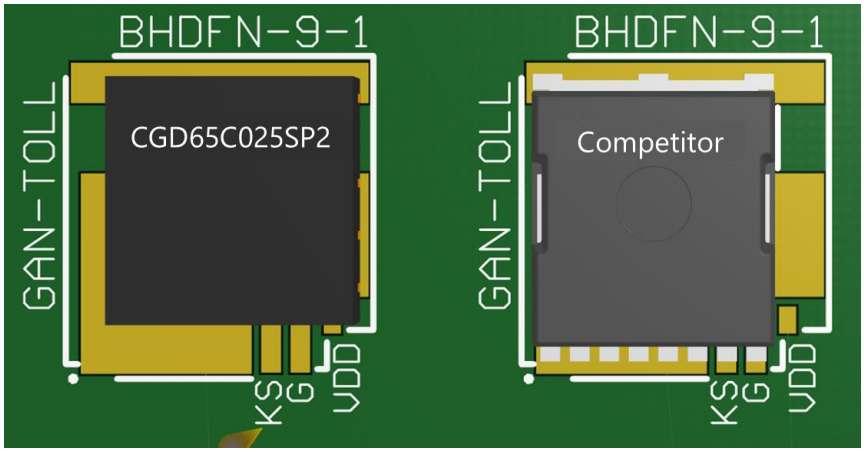


Figure 6 – PCB view of BHDFN & TOLL packages positioned in a so called co-layout

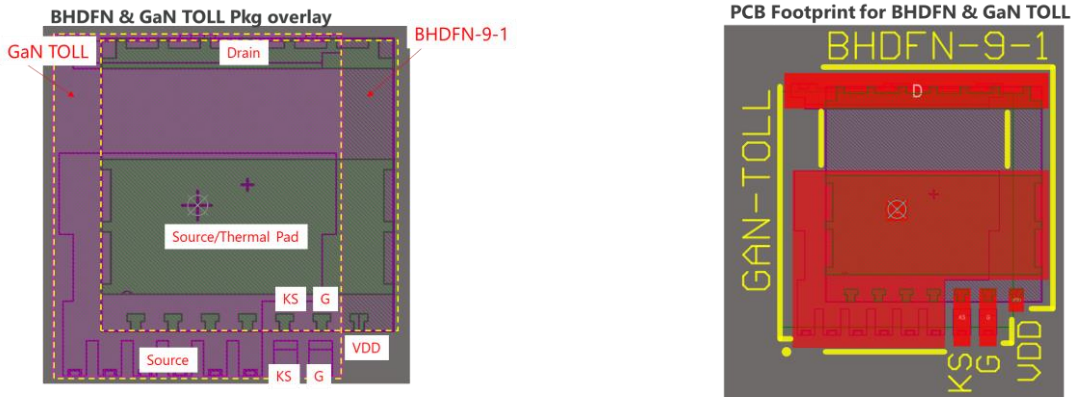
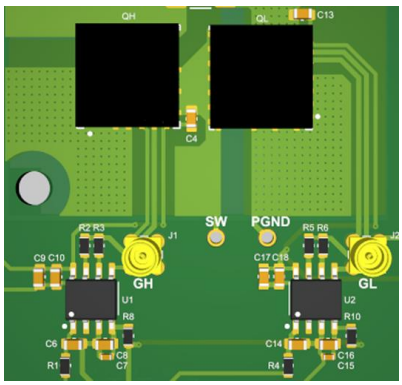


Figure 7 – (a) BHDFN & TOLL positions in the so called co-layout. (b) Red represents the co-layout copper pad

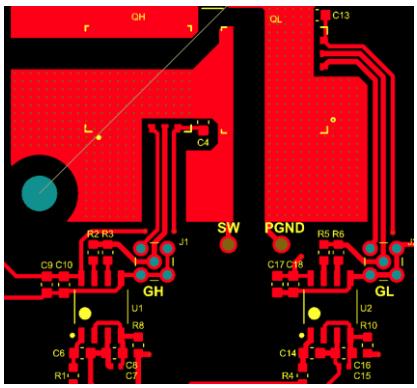
3.3 Example of effective thermal design layout in half-bridge configuration with drivers

PCB design involves considerations such as signal integrity, manufacturability, cost-effectiveness, thermal arrangement, and compliance with industry standards and regulations. The vast majority of high-power applications employ half-bridge configurations like TTPFC or LLC. In these topologies a compact switching node is essential for generating low noise and minimizing electromagnetic interference (EMI). To make the switching node as short as possible to minimize parasitic inductance and maximize the thermal pad area, one option could be to rotate the low-side devices by 90 degrees anticlockwise. This configuration ensures a short path from the low-side drain to the high-side source and facilitates the extension of the thermal pad for both devices to enable efficient heatsink assembly. Moreover, both source terminals allow ample area to accommodate thermal vias, further enhancing heat dissipation capabilities. Additionally, thanks to the internal Miller Clamp of ICeGaN devices, they exhibit significantly higher immunity to high dv/dt events compared to discrete GaN, thereby drastically reducing the effects of gate loop parasitic. This feature provides more flexibility in the placement of external driving SMD components.

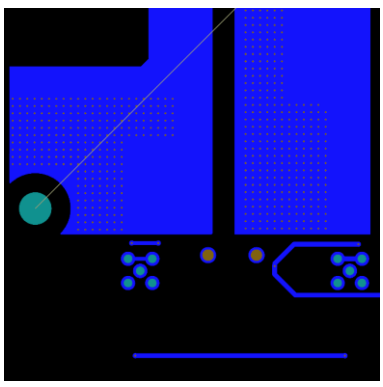
An example PCB design is shown in Figure 8. This daughter card has been specifically engineered for a 3-kW totem-pole PFC application to minimize parasitic elements and optimize thermal dissipation. This example is a 2-layer PCB design but can easily be replicated in a design that requires more layers. The low-side ICeGaN is rotated 90 degrees anticlockwise, noted by a pin-1 white dot in Figure 8(a). Moreover, by placing the VDD capacitors near their corresponding ICeGaN devices while positioning the gate resistors at a relatively greater distance, additional space is created. This surplus space facilitates the expansion of the thermal pad area and increases the number of vias, enhancing overall thermal management and mitigating thermal resistance, critical factors for robust performance in high-power applications.



(a) 3D Altium image top view



(b) PCB top layer



(c) PCB bottom layer

Figure 8 – Half-bridge layout example with ICeGaN in BHDFN package

4 Thermal measurements

4.1 Thermal evaluation environment

BHDFN, like TOLL, is a surface-mounted device and the assembly involves mounting the package onto a PCB, typically FR-4, with an external heatsink connected to the board's rear surface via a TIM sheet. The PCB requires copper vias to transfer the heat from the case thermal pad, the source terminal, to the heatsink.

Thermal evaluation was conducted to compare CGD65C025SP2, in a BHDFN package, with two GaN competitor parts in a TOLL package.

Taking advantage of the co-layout approach outlined in section 3.2, a PCB was designed to facilitate testing of both packages under the same conditions. The PCB incorporates many vias to minimize the thermal resistance within the PCB itself. Figure 9 depicts the PCB and heatsink assembly used for the thermal testing; Figure 10 is a PCB-design screenshot of the thermal pad area that was replicated in the 4 layers. Figure 11 are pictures of the actual board; It shows the top view of the PCB and detail of the thermal pad present in both the top and bottom layers. The white square line on top side indicates the heatsink position on the back of the PCB. By employing the same thermal interface material and an identical heatsink setup with air cooling, we aimed to ensure consistent test conditions. This design choice allows us to have the lowest R_{thJC}, for a more accurate and fair comparison of the thermal performance between the two packages under the same conditions.

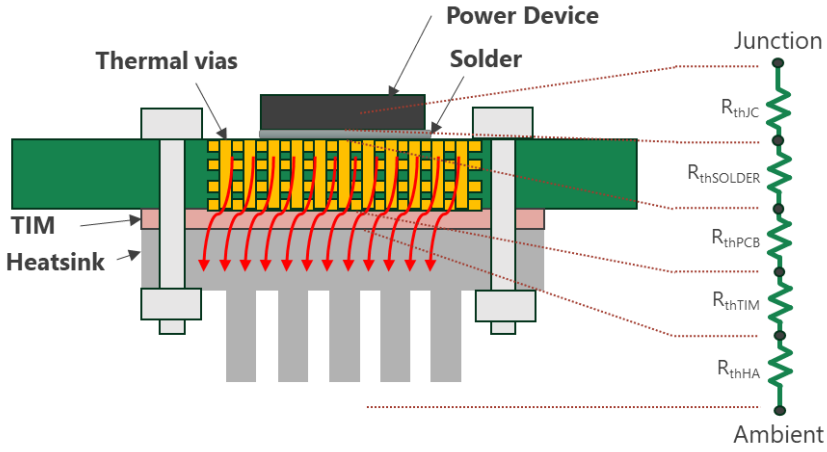


Figure 9 – Mounting of the PCB designed for thermal evaluation

The board is a 4-layer FR-4 PCB with 2oz copper layer. The thermal vias were 12 mil (0.3 mm) diameter placed on 25 mil (0.64 mm) grid spacing with 1 mil (25 µm) via plating.

	CGD BHDFN	GaN TOLL
PCB thermal pad area	185 m^2	185 m^2
Thermal-pad area under the device	45 m^2	49 m^2
Total vias in PCB thermal pad area	414	414
Vias under the device	144	161

Table 2 – Thermal pad dimensions and number of vias in the PCB for thermal evaluation

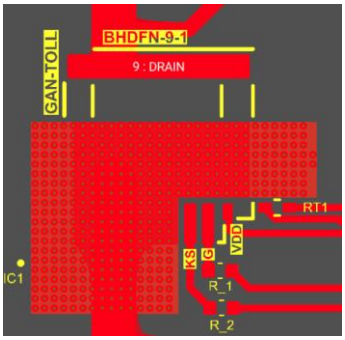
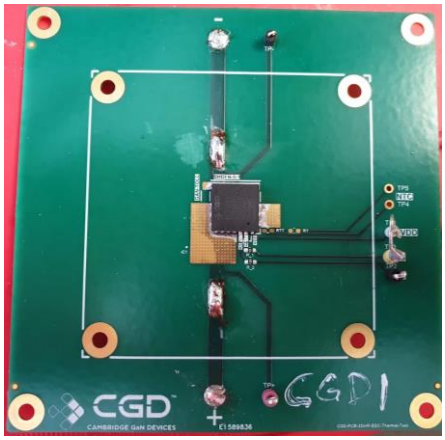
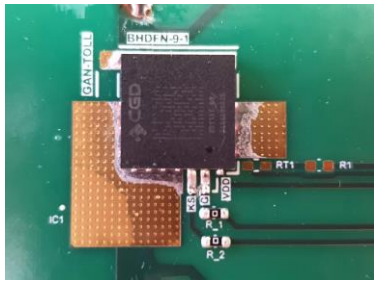


Figure 10 – PCB thermal pad design for the thermal evaluation



(a)



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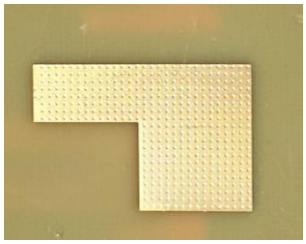


(c)

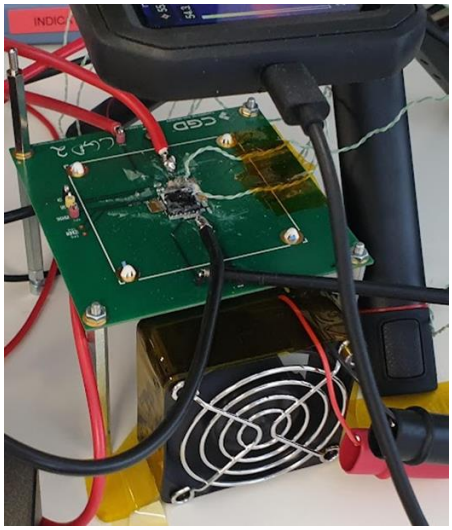
Figure 11 – (a) Test PCB with a CGD65C025SP2 assembled. (b) Thermal-pad top view detail. (c) Thermal-pad bottom view detail.

The TIM employed was Thermal foil 1500ST Sil-Pad® 1500ST with 0.23 °C-in^2/W thermal impedance, and the aluminium heatsink chosen was Wakefield Thermal Heat Sink Aluminium 60mm x 21mm - SKV606021-AL with a 0.9 °C/W natural thermal resistance with airflow.

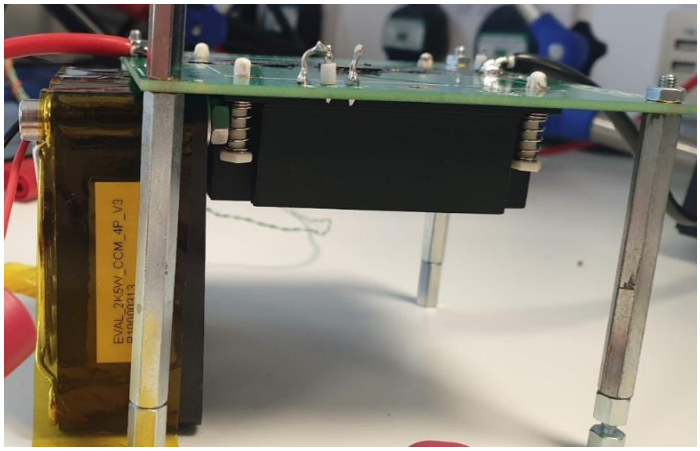
To validate T_J on the devices, we employed $R_{DS(on)}$ as electrical parameter to measure T_J. $R_{DS(on)}$ was characterised in the thermal chamber at different temperatures and operating in forward conduction at I_{DS}=1 A and the recommended V_{GS}. Thermal camera and K-type thermocouples were also employed for a reassurance as second source to validate each measurement.

4.2 BHDFN vs TOLL benchmark – R_{thJA}

To assess the heat dissipation and compare the devices across the 2 packaging types, the devices were operated in forward conduction at the respective recommended V_{GS} settings. A DC power supply in constant power mode was used to heat the devices.

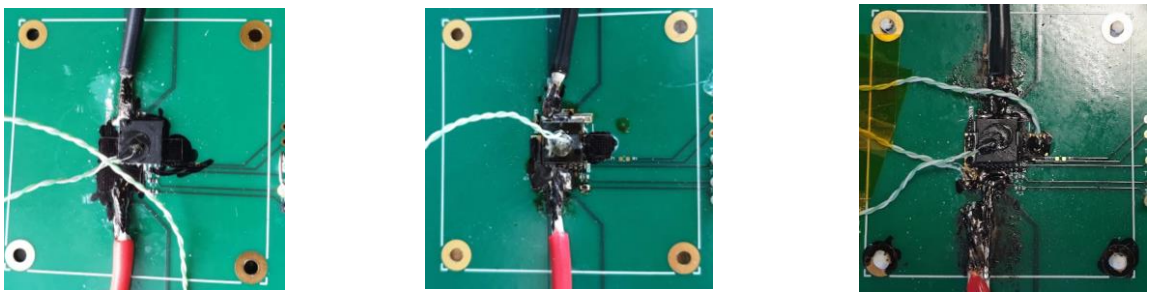


(a)



(b)

Figure 12 Thermal test set-up



(a) *(b)* *(c)*

Figure 13 – (a) CGD65C025SP2 in BHDFN package; (b) and (c) are TOLL-package GaN competitors

Figure 12 shows the test set-up employed for the three devices under test. During the test this set-up was enclosed in a plastic box to keep the ambient temperature unchanged. Figure 13 shows the three devices that were tested mounted on their respective PCBs.

The benchmarking results, presented in Table 3 and Figure 14 demonstrate comparable thermal performance of ICeGaN in a BHDFN package and GaN competitors in a TOLL package. These values were calculated using the TJ measured using $R_{DSON(TJ)}$ characterisation made in a thermal chamber.

Under these test conditions at T_{amb} = 25 °C and 20-W power dissipation T_J of both TOLL and BHDFN is approximately at 87 °C in the three devices. The difference between them in temperature is less than 1 °C.

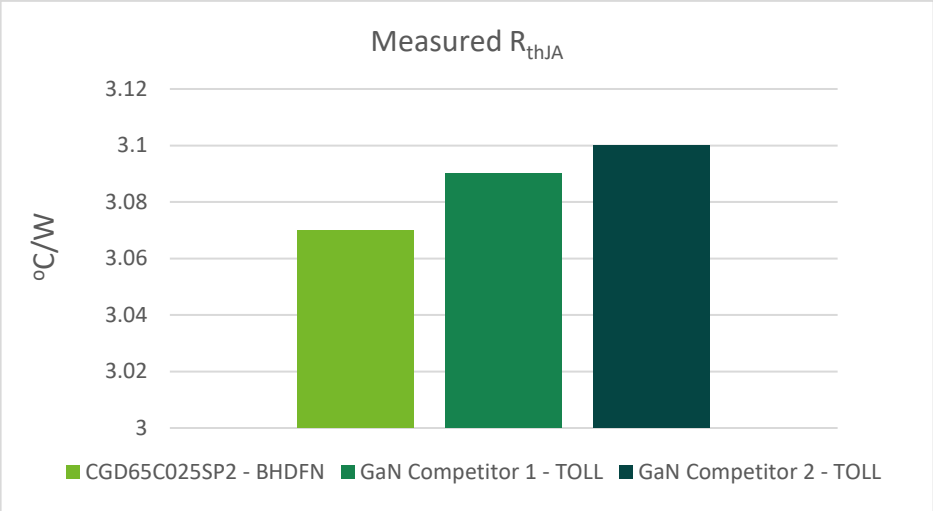


Figure 14 – R_{thJA} comparison, BHDFN CGD65C025SP2 and TOLL GaN competitors

DUT	Footprint / Layout	R_{thJA} Measured °C/W
CGD65C025SP2	Common layout BHDFN/TOLL (GaN)	3.07
Competitor 1	Common layout BHDFN/TOLL (GaN)	3.09
Competitor 2	Common layout BHDFN/TOLL (GaN)	3.1

Table 3 – R_{thJA} values of BHDFN CGD65C025SP2 and TOLL GaN competitors

5 Conclusion

CGD's BHDFN package provides outstanding thermal performance, making it highly suitable in high-power applications. Its 5-terminal, 9-pin configuration includes a large source-pin thermal pad, wettable flanks for easy inspection, and a thick lead frame for efficient heat dissipation. In addition, a common layout with TOLL package allows easy evaluation of CGD's BHDFN products. Comparative thermal tests against the TOLL package affirm that the BHDFN's performance is on par with the TOLL package, highlighting its suitability for demanding applications where efficient heat management is critical.

References

[1] "CGD-AN 2302 - How to use ICeGaN" May 2024. [Online]. Available: https://cms.camgandevices.com/uploads/AN_2302_How_to_use_I_Ce_Ga_N_0ac6f44376.pdf

[2] "ICeGaN™ - A Novel Technology for Integrated Power GaN" Mar 2022. [Online]. Available: https://cms.camgandevices.com/uploads/CGD_WP_2201_A_Novel_Technology_for_Integrated_Power_Ga_N_422664c9cc.pdf

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Revision History

Revision Number	Comments	Engineer(s)	Date
1.0	Initial Release	CT	2024-06-18
1.1	™ replaced by ® in the title ICeGaN footprint updated (Figure 4, Figure 5);	CT	2024-08-28
1.2	Minor grammar corrections	DSM	2025-05-13

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