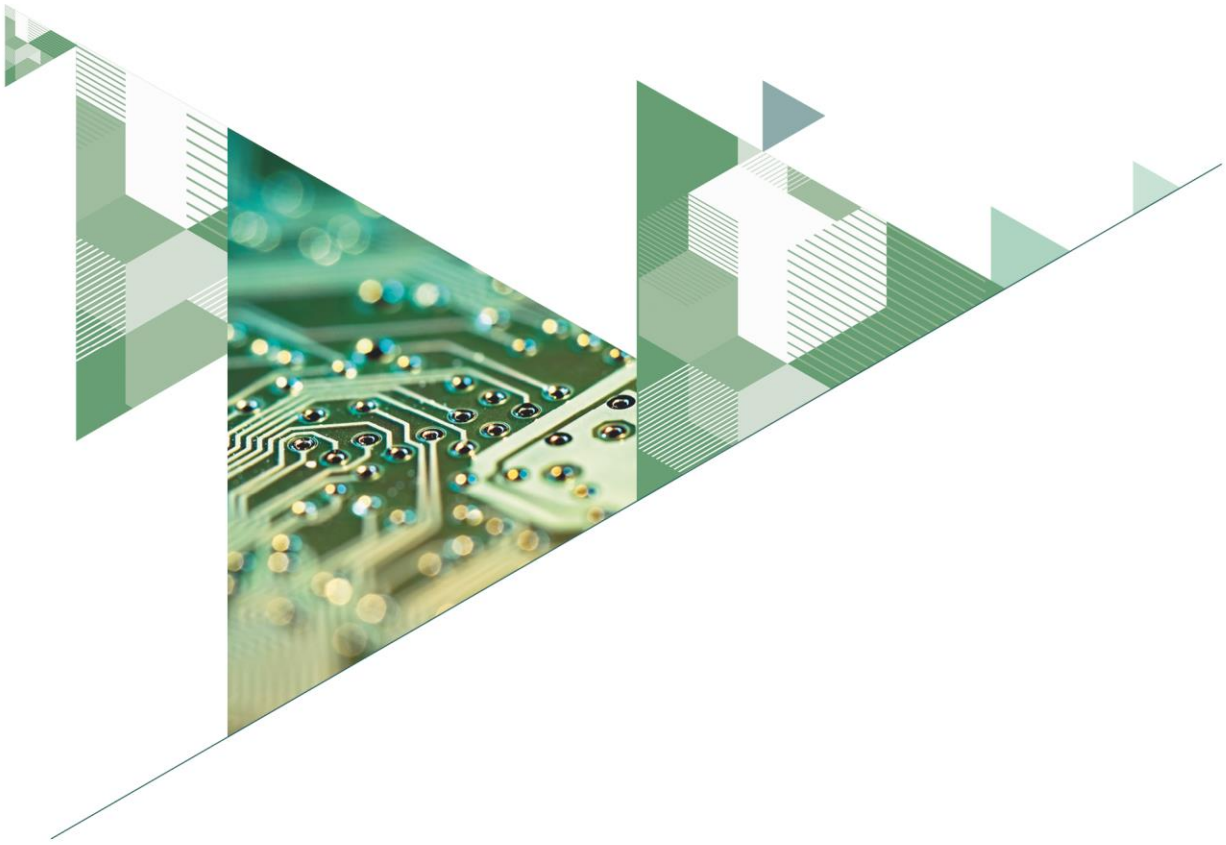


# CGD65B130S2
# DATASHEET

## 650V / 130 mΩ GaN HEMT with ICeGaN™ Gate and Current Sense

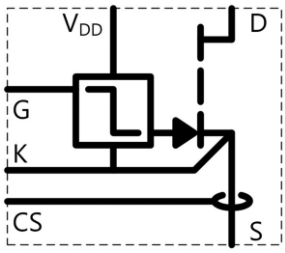
MARCH 2022

CAMBRIDGE GaN DEVICES

# 650V / 130 mΩ GaN HEMT with ICeGaN™ Gate and Current Sense

## Key features

- 650 V - 12 A e-mode GaN power switch
- ICeGaN™ gate technology for high gate threshold and broad gate voltage window compatible with gate-drivers for Si MOSFETs
- Gate drive voltage 9 V to 20 V
- Current sense function
- $R_{DS(on)}$ = 130 mΩ
- Suitable for very high switching frequency
- Kelvin Contact
- Small 5x6 $mm^2$ PCB footprint
- Bottom side cooled DFN package





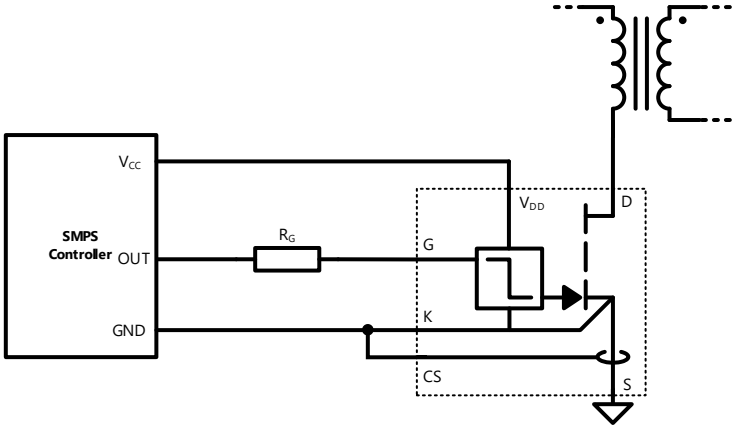
## Description

The CGD65B130S2 is an enhancement mode GaN-on-silicon power transistor, exploiting the unique material properties of GaN to deliver high current, high breakdown voltage and high switching frequency for a wide range of electronics applications. The CGD65B130S2 features CGD's ICeGaN™ gate technology enabling compatibility with virtually all gate drivers and controller chips available. The integrated current sense function eliminates a separate current sense resistor and the associated efficiency losses. Because no external sense resistor is needed, the device can be directly soldered to the large copper area of the ground plane, improving the thermal performance and simplifying the thermal design. It comes in a DFN 5x6 SMD package to support high frequency operation while ensuring the highest thermal performance.

## Application & Topologies

PSUs, Industrial SMPS and inverters

- Server power and data centres
- Telecom rectifiers
- Gaming PSUs
- PC power
- LED drivers
- High power ClassD Audio
- General purpose SMPS
- PV inverters
- SMPS and converters in single-switch and half-bridge topologies with hard- or soft-switching
- AC/DC and DC/DC converters
- Totem pole and single-switch PFC
- AC inverters
- Forward, flyback and LLC converters at high frequency




*Exemplary Application Circuit*

## Absolute Maximum Ratings

$T_{case}$ = 25 °C if not listed.

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| Operating Junction Temperature | $T_J$ | -55 to +150 | °C |
| Storage Temperature Range | $T_S$ | -55 to +150 | °C |
| Drain-to-Source Voltage | $V_{DS}$ | 650 | V |
| Drain-to-Source Voltage - transient [1] | $V_{DS}$ | 750 | V |
| Gate-to-Source Voltage | $V_{GS}$ | -1 to +20 and $V_{GS} \leq V_{DD}$ | V |
| Gate-to-Source Voltage - transient | $V_{GS(transient)}$ | -1.5 to +21.5 and $V_{GS} \leq V_{DD}$ + 1.5 | V |
| ICeGaN™ Gate Supply Voltage | $V_{DD}$ | 0 to +20 | V |
| Continuous Drain Current ($T_{case}$= 25 °C) | $I_D$ | 12 | A |

The range of operation for $V_{GS}$ and $V_{DD}$ is 9 V to 20 V, enabling simple integration with a large variety of control chips and gate drivers.

[1] Non-repetitive pulsed conditions.

## Electrical Characteristics

Values at $T_J$ = 25 °C, $V_{DD}$ = 12 V if not listed. To turn the device on the recommended gate voltage range is $V_{GS}$ = 9 V to $V_{DD}$. To turn the device off set $V_{GS}$ = 0 V. An integrated Miller Clamp eliminates the need for negative gate voltages.

### STATIC CHARACTERISTICS

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Drain-to-Source Blocking Voltage | $BV_{DS}$ | $V_{GS}$ = 0 V, $I_{DSS}$ = 8.5 µA | 650 | | | V |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 12 V, $I_D$ = 0.9 A | | 130 | 182 | mΩ |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 12 V, $I_D$ = 0.9 A | | 350 | | mΩ |
| Source-to-Drain Voltage | $V_{SD(on)}$ | $V_{GS}$ = 0 V, $I_D$ = 0.9 A | | 2.0 | 2.6 | V |
| Gate-to-Source Threshold | $V_{GS(th)}$ | $V_{DS}$ = 0.1 V, $I_D$ = 4.2 mA | 2.3 | 2.9 | 3.5 | V |
| Gate-to-Source Threshold | $V_{GS(th)}$ | $T_J$ = 150 °C<br>$V_{DS}$ = 0.1 V, $I_D$ = 4.2 mA | | 2.6 | | V |
| Gate-to-Source Current | $I_{GS}$ | $V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 2.8 | 3.7 | mA |
| Gate-to-Source Current | $I_{GS}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 2.5 | | mA |
| $V_{DD}$ current | $I_{VDD}$ | $V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 1.8 | 2.8 | mA |
| $V_{DD}$ current | $I_{VDD}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 1.1 | | mA |
| Drain-to-Source Leakage Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | 0.2 | 8.5 | µA |
| Drain-to-Source Leakage Current | $I_{DSS}$ | TJ = 150 °C<br>$V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | 12 | | µA |

### DYNAMIC CHARACTERISTICS

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Output Capacitance | $C_{OSS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V<br>f = 100 kHz | | 25 | | pF |
| Output Charge | $Q_{OSS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V | | 25 | | nC |
| Total Gate Charge[2] | $Q_G$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0...12 V<br>$I_D$ = 4.2 A, $I_G$= 15 mA | | 2.3 | | nC |
| Reverse Recovery Charge | $Q_{RR}$ | $I_S$ = 8 A, $V_{DS}$ = 400 V | | 0 | | nC |
| Turn-on delay time | $t_{d(on)}$ | See Figure 15 and Figure 16 | | 6 | | ns |
| Turn-off delay time | $t_{d(off)}$ | See Figure 15 and Figure 16 | | 20 | | ns |
| Rise time | $t_r$ | See Figure 15 and Figure 16 | | 6 | | ns |
| Fall time | $t_f$ | See Figure 15 and Figure 16 | | 6 | | ns |

[2] Turn-on gate charge value is listed. Turn-off gate charge value is lower, because ICeGaN™ discharges the gate internally.

## CURRENT SENSING

Please refer to the application note CG-AN2206: Current Sensing with ICeGaN™. Please contact CGD for advice on the use of the current sense function.

## ESD RATING

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ESD withstand rating | HBM | Human Body Model (per JEDEC JS-001-2017) | 2000 | | | V |
| ESD withstand rating | CDM | Charged Device Model (per JEDEC JS-002-2018) | 1000 | | | V |

## Thermal Characteristics

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Thermal resistance, junction to case | $R_{th(JC)}$ | | | 2.3 | | K/W |
| Reflow soldering temperature | $T_{reflow}$ | MSL3 | | | 260 | °C |

## Figures

Figures at $T_J$ = 25 °C, $V_{DD}$ = 12 V if not specified.

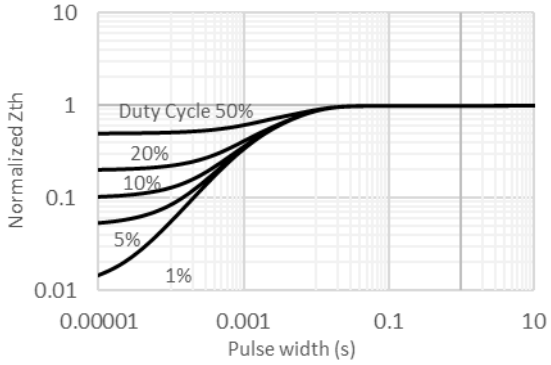



*Figure 1. Normalized thermal transient impedance ($Z_{th,JC}$) as a function of pulse width.*

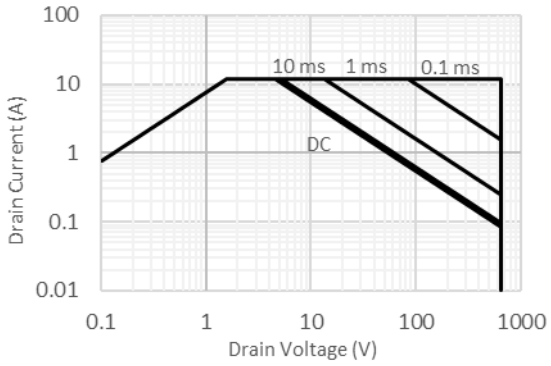



*Figure 2. Safe Operating Area (SOA) based on thermal impedance $Z_{th,JC}$ at $T_{CASE}$ = 25 °C.*

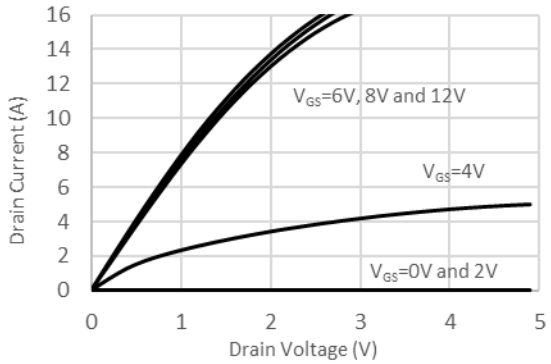



*Figure 3. Forward output characteristics at $T_J$ = 25 °C.*

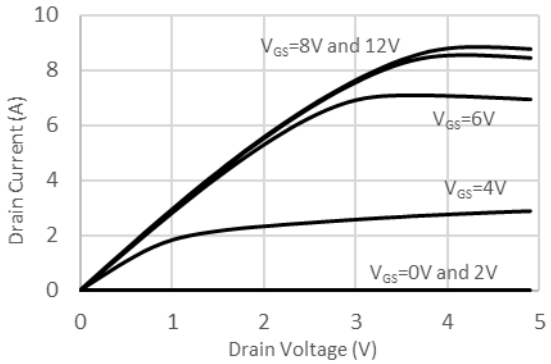



*Figure 4. Forward output characteristic at $T_J$ = 150 °C.*

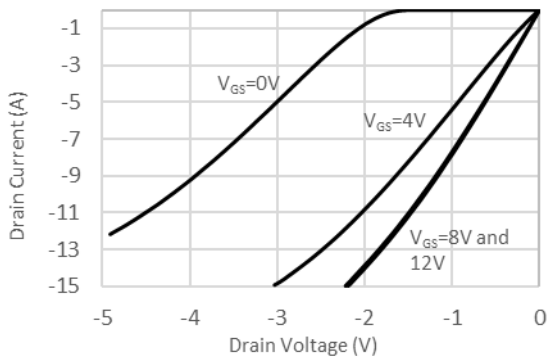



*Figure 5. Reverse output characteristics at $T_J$ = 25 °C.*

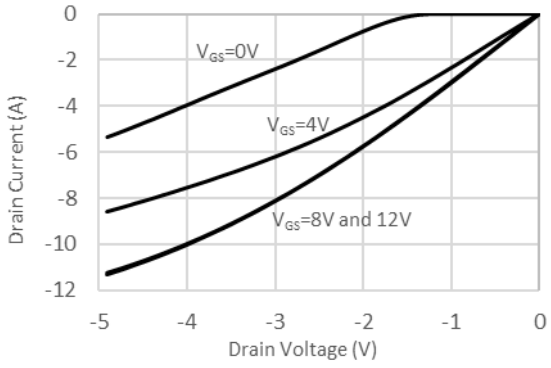



*Figure 6. Reverse output characteristics at $T_J$ = 150 °C.*

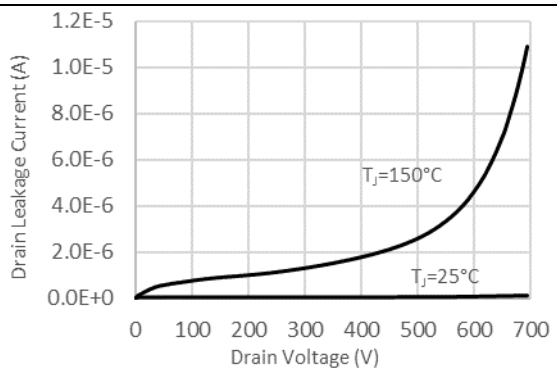



*Figure 7. Drain leakage current characteristics at $T_J$ = 25 °C and $T_J$ = 150 °C.*

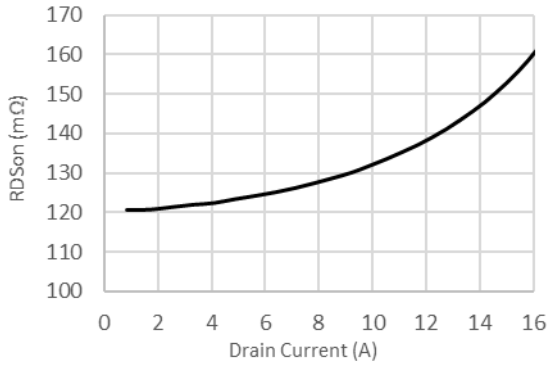



*Figure 8. On-state resistance as a function of drain current at $T_J$ = 25 °C.*

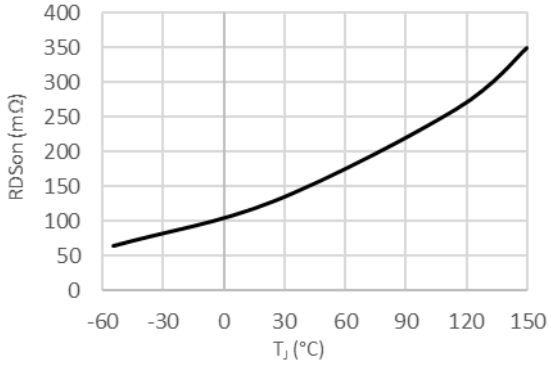



*Figure 9. On-state resistance as a function of junction temperature at $V_{GS}$ = 12 V.*

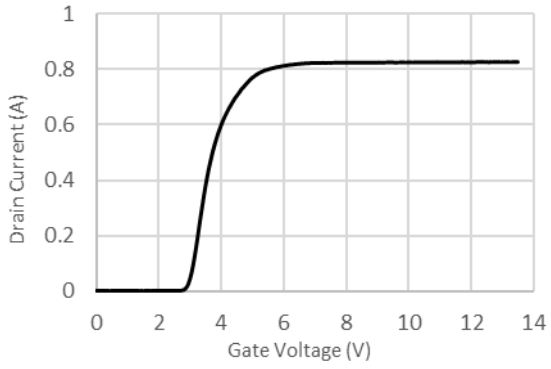



*Figure 10. Transfer characteristics at $V_{DS}$ = 0.1 V, $T_J$ = 25 °C.*

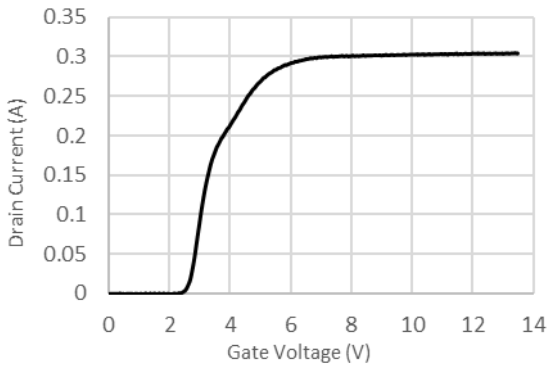



*Figure 11. Transfer characteristics at $V_{DS}$ = 0.1 V, $T_J$ = 150 °C.*

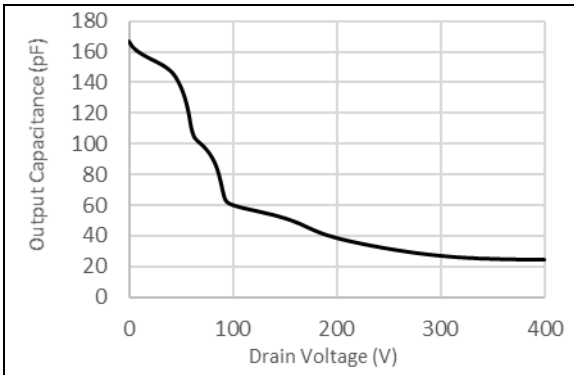



*Figure 12. Typical output capacitance $C_{OSS}$ vs. $V_{DS}$ at 100 kHz, $T_J$ = 25 °C.*

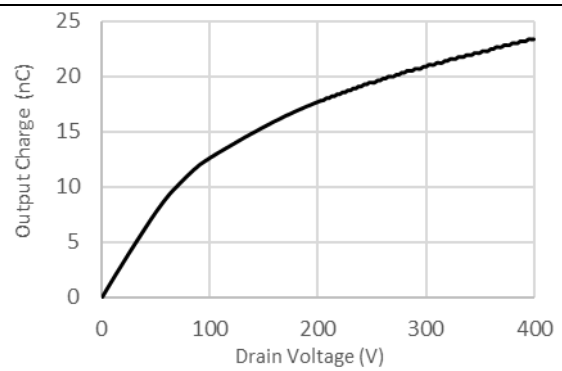



*Figure 13. Typical output charge $Q_{OSS}$ vs. $V_{DS}$ at 100 kHz, $T_J$ = 25 °C.*

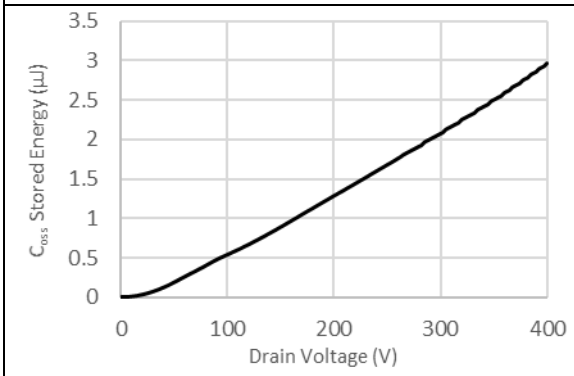



*Figure 14. Typical $C_{OSS}$ stored energy $E_{oss}$ vs. $V_{DS}$ at $T_J$ = 25 °C.*

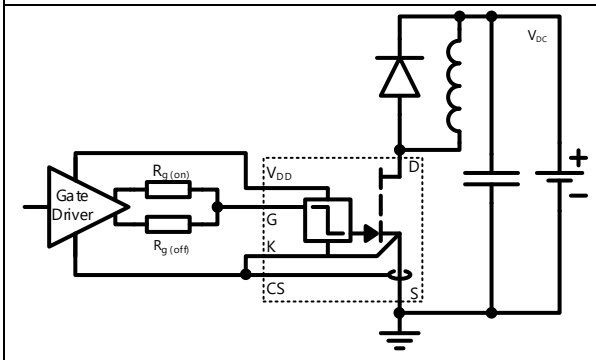



*Figure 15. Inductive switching circuit. ID = 6 A, $R_{g(on)}$ = 15 Ω, $R_{g(off)}$ = 2 Ω, $V_{DD}$ = 12 V, $V_{DC}$ = 400 V, L = 125 µH, diode = IDH04G65C5.*

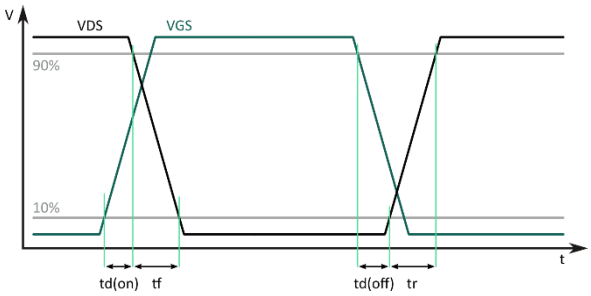



*Figure 16. Switching waveform timing definitions.*

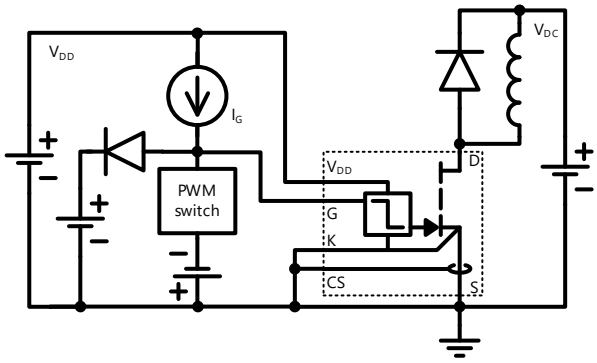



*Figure 17. $Q_G$ gate charge characterization circuit. $I_G$=15 mA, $V_{DC}$ = 400 V, $V_{DD}$=12V, L = 125 µH, freewheeling diode = IDH04G65C5.*

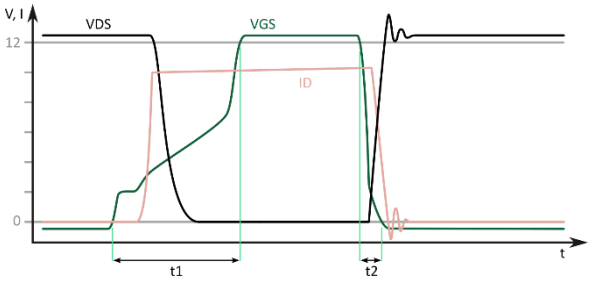
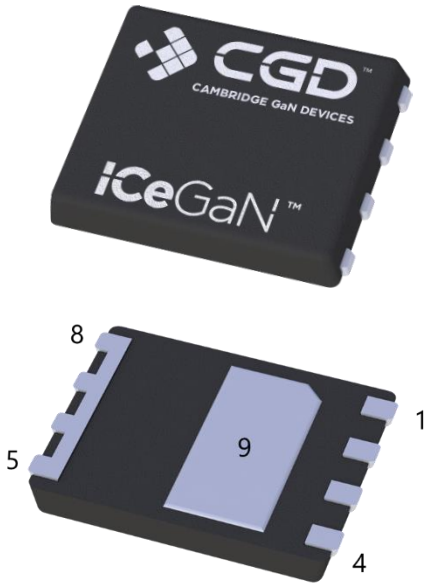


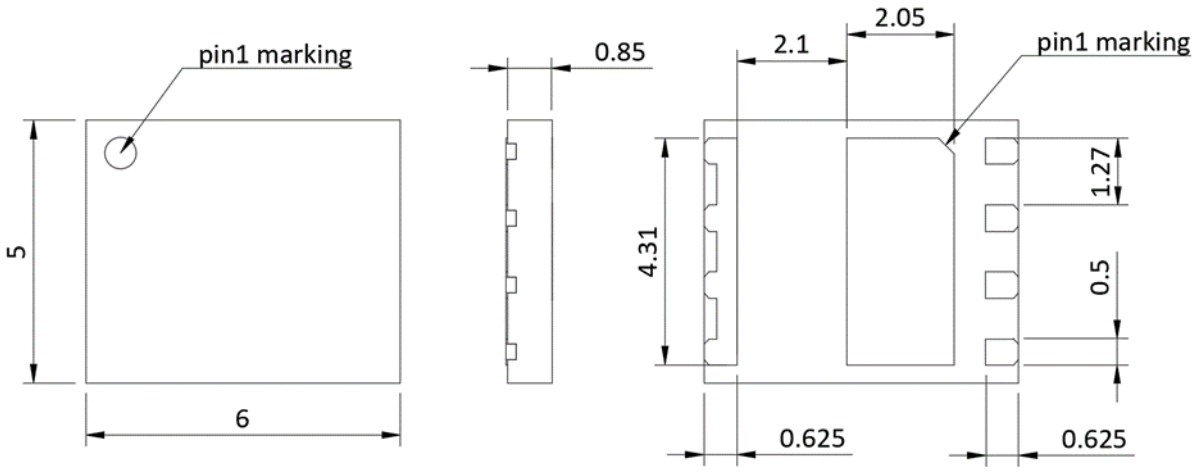

*Figure 18. $Q_G$ gate charge characterisation waveform at $I_G$ = 15 mA and $V_{DD}$ = 12 V. Time intervals t1 and t2 indicate the integration boundaries to calculate $Q_G$ from $I_G$ at turn-on and turn-off. Turn-off gate charge is lower than turn-on gate charge.*

## Packaging

DFN 5x6 mm.

| PIN NUMBER | NAME |
|---|---|
| 1 | Kelvin |
| 2 | Gate |
| 3 | Current Sense |
| 4 | $V_{DD}$ |
| 5-8 | Drain |
| 9 | Source |




### Version History

This version is 1.0

| VERSION | DESCRIPTION | DATE | BY |
|---|---|---|---|
| 1.0 | Initial Release | March 2022 | MA, AB, JZ |

*Dare to innovate differently*

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